Design for Excellence (DFX)

Driving Product Optimization Through Early Stage Supplier Engagement

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SMTC Corporation

- Established in 1985
- Over 600,000 square feet of manufacturing capability
- Facilities that covers a large global footprint
- More than 40 manufacturing and assembly lines
- Approximately 1,300 employees
- Listed on NASDAQ since 2000 (SMTX)
- Frost & Sullivan Awards Winners – Growth Leadership and Product Quality Leadership Awards

Our Vision
To simplify the lives of our customers by delivering extraordinary Customer Service, Responsiveness, Quality, Technology Solutions and Value, fueling their Success and Our growth

Our Values
- Solution Oriented
- Collaborative Partner
- Professional integrity
- Proactive
- Innovative
- Dependable
Medical Device Markets

Specialists in the Design and Manufacture of Complex Class I and II Medical Devices

We design and manufacture class I and II medical devices that require a mix of highly specialized technologies including:

- Diagnostic devices
- Imaging equipment
- Laboratory equipment
- Patient Monitoring systems
- Infusion Pumps
- Dispensing Systems
- Consumer Wellness Products.
DFX Product Optimization

- What is DFX?
- DFX Benefits
- Product Value Equation
- Ability to Impact Product Value
- Early Supplier Involvement (ESI)
- Product Development
  - dFMEA
  - Design for Reliability (DFR)
  - Design for Supply Chain (DFSC)
- High Level Design
  - Design for Testability (DFT)
- Physical Design
  - PCB Design Engagement
  - Design for Assembly (DFA)
  - Design for Reliability (DFR)
  - Design for Fabrication (DFF)
  - Design for Testability (DFT)

Prototype
  - Design for Manufacturing (DFM)

Validation
  - Design for Reliability (DFR)

New Product Introduction
  - FMEA and Control Plan

Production

ESI Benefits
What is DfX?

- **DFX** or **Design for eXcellence** is the application of Rules, Guidelines and Methodologies during the Product Development with the purpose of impacting it’s **Value** while meeting the Product Design Requirements.
- The **x** in Dfx represents an aspect of the product value to be targeted; these may include (*but not limited to*)
  - **Design for Supply Chain (DFSC)**
    - Process of ensuring material sourcing, supply, compliancy and lifecycle requirements are met during design stage.
  - **Design for Reliability (DFR)**
    - Process for ensuring reliability of a product or system during the design stage *before* physical prototype
  - **Design for Fabrication (DFF)**
    - Process of ensuring the manufacturability of the PCB fabrication design and related cost drivers are met.
  - **Design for Assembly (DFA)**
    - Process of ensuring the assembly of the PCB design and physical layout rules are met prior to prototype
  - **Design for Manufacturability (DFM)**
    - Process of ensuring the manufacturability of a component or complete assembly to met supplier’s capability.
  - **Design for Test (DFT)**
    - Process of analyzing test access, coverage and schematics are designed for test
DFX Benefits

- **Product Design for Manufacturability**
  - Improved PCB yield, performance and cost *(DFF)*
  - Improved Assembly yield and reduced labour content *(DFA)*

- **Product Design for Testability**
  - Improved Coverage, Reliability and Final yield, reduced RMA and field failures. *(DFT, DFR)*
  - Reduced development engineering resource commitment, improved time to market

- **Product/ Process Stability and Repeatability**
  - Reduced lead time, improved availability/lifecycle and material costs *(DFSC)*
  - High quality, reliable and robust performance for the life of the product *(DFR)*

- **Capability**
  - Improved Production Stability and Predictability *(DFM)*

- **First Pass Yield and Capacity**
  - Continuous Improvement *(DFM)*
Product Value Equation

**PERFORMANCE**
Performance can be a function, need, feature or aspect that is deemed critical to the product design.

**COST**
Cost can include material, labor, test, logistics or any other aspect required to provide the required performance.

**VALUE**
Ability to Impact Product Value

80% of Product’s Recurring Cost Established

TYPICAL PRODUCT DEVELOPMENT CYCLE

ABILTY TO IMPACT

ARCHITECTURE
- Component selection – Major (e.g. Processor)
- Hardware / Software partitioning

HIGH LEVEL DESIGN
- Schematic Design
- ASIC/FPGA Design
- Component Selection

PHYSICAL DESIGN
- PCB Layout
- DFM
- DFT
- Component Selection (e.g. passives)

Prototype
- Quick Turn Prototype
- Early DFM/DFT Feedback

VALIDATION
- Device level testing
- System integration testing
- EMC testing
- Agency submissions

NPI
- Supply chain tweaking

VOLUME
- Continuous process improvement

30% of NPI Cost Established

DFEM – Design for Manufacturability

DFF – Design for Fabrication

DFA – Design for Assembly

DFT – Design For Test

DFSC – Design For Supply Chain

DFR – Design For Reliability

DFX ENGAGEMENT

TYPICAL PRODUCT DEVELOPMENT CYCLE

COSTED ACTIVITIES

Strictly Confidential [Rev. July 2015]
Early Supplier Involvement (ESI)

Common Development Mistakes
1. Lack of Collaboration and Review of Requirements
2. Poor understanding of supplier capabilities/limitations
3. Customer expectations (reliability, lifetime, use environment) are not incorporated into the new product development

Best Practice
- Early supplier involvement in the product design cycle can provide customers with a product that is more cost effective, increased manufacturability and quality, has higher reliability and longer overall lifecycle.
- Design reviews at key stages throughout the design cycle provides critical feedback to address potential issues to ensure a successful new product introduction and high quality, high yielding, reliable and manufacturable product.
Product Development

Architecture/ Concept Key Activities

- Selection of Critical Components
- Defining Environment Requirements
- Detailed Specifications
- Hardware/ Software Requirements
- Defining Key Functions/ Features

Supplier Engagement

- Major Component Suppliers
- Manufacturer
- Supply Chain/ Procurement

DFX Review

- Design for Reliability (DFR)
  - Critical Component Selection
  - Desired Lifetime/ Environment
  - PCB Design Considerations
- Design for Supply Chain (DFSC)
  - Predicted Lifecycle and Sourcing
  - Process Compatibility
  - Strategic Supplier Alignment
Impact of Design Decisions

- Although very early in the design cycle, key component suppliers should be providing their component level dFMEA, reliability and design suitability input.

- Reliability and Lifetime decisions made now will be very difficult to change later in the design cycle. A thorough design review should be made.

- Sourcing and strategic alignment of the supply chain and a predicted EOL should be reviewed.

- Specifying a custom single sourced processor slated to go EOL can limit component availability, time to market and potentially require a complete redesign.
Design for Reliability (DFR)

DFR is performed early in the design cycle to identify approved manufacturer part numbers which for reasons of lifecycle, availability, process compatibility or validity are addressed prior to initial design.

- **Critical Component Considerations**
  - Sensitivity of the circuit to component performance
  - Number of components within the circuit
  - Output from FMEA (Failure Mode Effects Analysis)
  - Historical experience/Industry data
  - Component technology
  - Tin Whiskers
  - Ceramic Capacitor (Cyclic Voltage)
  - Resistors (High Resistance - SIR)
  - Thick Film Resistors (Sulfide Corrosion)
  - Electrolytic Capacitors
  - Connectors
  - Wear Out – Memory, Relay/Switches/LED

- **Desired Lifetime**
  - Temperature/Humidity/Electrical Load/Vibration/Mechanical Stress/Shock/Power Cycling

- **PCB Design**
  - Surface Finish - OSP, ENIG, HASL, Immersion Silver
  - Stack up, Laminate (Tg/Td), Blind/Buried Vias, Microfill/Plating
  - Land Pattern Design, Spacing, Voltage Bias
  - ICT Stress
Design for Supply Chain (DFSC)

DFSC performed early in the design cycle helps to identify selected manufacturer part numbers which for reasons of lifecycle, availability, process compatibility or validity are addressed prior to initial design.

- **BOM Health Check**
  - Review AML data for completeness (orderable) and preferred supply.
  - Ensure MPN match with part description
  - Hazardous Substance Content
  - Manufacturing Process Compatibility

- **BOM Lifecycle Analysis**
  - Form-Fit-Function (FFF) replacement reviews
  - Predicted Lifecycle and YTEOL Forecasts
  - Change Notices and Counterfeit Alerts

- **Value Add**
  - AML Expansion and Preferred supplier selection
  - Supply Chain Optimization
  - EOL and Alternate Qualification
  - Cost Reduction
A BOM Health Analysis services can be performed utilizing leading providers of component information on the global market and economy.

Advanced reporting tools and prediction services can provide insight on Risk and make informed decisions prior to securing the architecture.

**Health Analysis**

- Provides an overall health of the BOM supply chain based on current and predicted lifecycle, available sources and compliancy.

- **AML**
  - Total AML: 7883
  - Total Active AML: 5093

- **Risk:**
  - Discontinued w/o Alts: 142
  - Discontinued with Alts: 498
  - EOL: 26
  - Single Sourced: 1860
  - RoHS Non-Compliant: 87

- **Calculated Health Score:**
  - 612.6 out of a possible 1000
BOM Analysis

- BOM Analysis provides insight to identifying opportunities and focus to improve supply chain health and AML alternates to address single sourced, EOL/Discontinued, Non-compliant and address material cost drivers.

- **Risk Areas**
  - Discontinued AML: 498 w/ alt, 143 w/o alt.
  - EOL AML: 26
  - Non-compliant: 86
  - Single Sourced AML - 1800

- **Value Add**
  - Evaluate FFF replacement recommendations or develop strategy to address Discontinued/EOL components.
  - Qualify RoHS equivalent orderable part numbers or provide alternates to address compliancy issues
  - Align strategic FFF AML Alternates to provide multiple sources to single sourced components.
  - Identify opportunities for cost reduction through FFF AML Alternate on existing AML.
  - Provide PCN support to proactively notify and address risk.
### AML Expansion

#### Project A

**Scope of the Project**

Targeting cost reduction, 40 parts were identified as FFF alternates to existing approved AML with a potential for 20% reduction in material costs. Cost avoidance of $38K was identified through alternate sourcing due to obsolescence.

**Value Engineering Services Implemented**

- Component Engineering

**Cost Savings**

- $126K

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#### Project B

**Scope of the Project**

Target cost reduction and in-plant store VMI for Power Supply for a potential 8% reduction in cost. Full functional part evaluation in system and test reports provided to support qualification.

**Value Engineering Services Implemented**

- Component Engineering

**Cost Savings**

- $87K
High Level Design

Hardware Design
- Schematic Design
- ASIC/ FBGA Design
- Cont’d Component Selection
- Hardware/ Software Requirements
- Defining Key Functions/ Features
- Test and Performance Definition

Who should be engaged?
- Supply Chain/ Procurement
- Software Engineers
- Test Development Partners
- Manufacturer

DfX Review
- Design for Testability
  - Schematic Review
  - Test Strategy Review
- Design for Supply Chain (DFSC)
  - Predicted Lifecycle and Sourcing
  - Process Compatibility
  - Strategic Supplier Alignment
Design for Testability (DFT)

- Early electrical design can be reviewed at the schematic level to identify electrical characteristics of the design that may have a negative impact on in-circuit test coverage or cost.

- Design rule and guidelines checks applied through advanced schematic modelling software can identify costly design errors at high level design.

- Advanced reporting provide comprehensive reports that highlight estimated production yield, test coverage by component, cycle times and validate early dFMEA assumptions.

- Adjustments to the schematic at this high level design to address access and design considerations including JTAG, Boundary Scan and related requirements can significantly reduce the overall cost and complexity of the test strategy.
Physical Design

- **PCB Design**
  - PCB Layout and Routing
  - PCB Stackup and Fabrication
  - Final Component Selection
    - Passives
    - Hardware
  - Design File Generation (Gerber, Fab, Placement)

Who should be engaged?
- PCB Designers
- Manufacturers
- PCB Fabrication
- Test Development Partners

DfX Review
- **Design for Assembly (DFA)**
  - Physical Layout
  - Assembly and Manufacturer
- **Design for Fabrication (DFF)**
  - Stack up and Impedance
  - PCB Fabrication Design Rules
- **Design for Testability (DFT)**
  - Nodal Analysis
  - Test Strategy Development
PCB Design Engagement

**Target Engagement**

- **Start**
- Week 2: Pre-placement
- Week 4: Placement
- Week 6: Routing
- Week 8: Verification
- Week 10: PCB FAB
- Week 12: PCBA production

**Typical Engagement**

- Too late to impact change

**Manufacturing**

- Pre-build review (Pre-DFM)
- BOM Analysis
- Assembly Analysis (Pre-DFA)
- Manufacturing review

**Routing**

- Assembly Analysis (DFA)
- PCB Fabrication Analysis (DFF)
- Test Access Analysis (DFT)
- ICT Pressure Analysis (FEA)
- 90% routing completion of tight sections
- # days TBD

**Verification**

- Gerber release
- # days TBD

**PCB Fabrication**

- Analysis

**Test Access**

- Analysis

**ICT Pressure**

- Analysis

**Manufacturing Post Build Review**

- Post-DFM

**Typical**

- Prototype shipment

**Target Engagement**

- Placement freeze
- 5 days

**Too late to impact change**

**BOM Analysis**

- Routing Verification

**PCBFAB**

- PCBA production

**PCBA Production**

- Manufacturing post build review (Post-DFM)

**Typically Too Late**

- Too late to impact change

# days TBD

**Typical Engagement**

- Placement freeze
- 5 days

**Too late to impact change**

**Prototype shipment**

**Typically Too Late**

- Too late to impact change

**Prototype shipment**
Design for Assembly (DFA)

- Design for Assembly targets opportunities in the physical layout of the assembly to identify areas for improvement and potential areas of concern to drive assembly cost out early in the design cycle.

- Rules and Guidelines are based on your manufacturers capabilities and component requirements.

- Design rules must be configured for your product requirements. i.e. Class 2 or 3, Reliability (Safety critical)

- Advanced software and combined with years of assembly experience. 500+ DFA checks can be performed to provide results on;
  - Component Analysis
  - Pad stack Analysis
  - Pin to Pad Analysis
  - Test Point Analysis
  - Solder Paste Analysis
Example DFA Output outlining Critical (Major), Hot (Yield improvement), Warm (Minor), Cool (No immediate concern) and Ignore (acceptable)
Design for Reliability (DFR)

- Design for Assembly Reports are an important tool to provide insight into Product failures
- Utilizing Six Sigma, estimated annualized cost avoidances can be assign to prioritize design change decisions.
- Analysis can be performed to address issues early in the design address potential reliability issues.

**Quality and Reliability Concern.**
2 OFE, 130 Locations – 260 Opportunities
Probability of Occurrence 50%
Expected Yield Detractor 2.5%
Rework Cost $2.80
**Potential Failure Cost $4,021.01**

**Quality and Reliability Concern.**
28 OFE, 14 Location – 392 Opportunities
Probability of Occurrence 40%
Expected Yield Detractor 0.72%
Rework Cost $0.42
**Potential Failure Cost $727.50**

**Quality and Reliability Concern.**
50 OFE, 2 Location – 100 Opportunities
Probability of Occurrence 50%
Expected Yield Detractor 0.23%
Rework Cost $0.70
**Potential Failure Cost $386.63**

Ref Des U37, U38, distance between pad too close (0.0059”). Prone to solder bridge. Recommend decreasing pad from 13.78 mil to 11 mils.

Ref R1050, C239, RN96, FB2, etc., masked trace between toe print is too thin, may break and cause insufficient solder. Minimum recommended clearance between exposed via and toeprint is 5mil.

Ref Des U48, U103, land pattern is not optimal, heel distance is too big. Too much heel may cause solder bridge under component, not visible to visual inspection. Recommended to decrease by 25 mil on heel side.
DFF is intended to help review customers' designs with respect to PCB manufacturability as early in the design cycle as possible, where it is easy to make decisions that drive out cost, improve fabrication yields and address concerns before final design is completed.

Reviews typically include determining workable stackups, including impedance trace widths.

Most supplier utilize automated DFX tools such as Valor to apply their internal Design Rule Checks (DRC) and will provide comprehensive DFM reports for Design Reviews.
**Design for Fabrication (DFF)**

- Suppliers will typically provide their DFM guidelines upon request.

- Incorporating these rules into your native Design Package can help drive value further up the Product Development Cycle.
Fabrication Panel Design

- Panel Design is a Primary Cost Driver for PCB
- % Utilization of the Master Panel will typically be the main cost
- Pushing ownership to the fabricator or manufacturer will have its PROS and CONS.

- It is important that both the fabricator and the manufacturer needs are taken into consideration and collaborative ownership of panel design should be carefully considered.
## PCB Cost

### Project A

**Scope of the Project**

Optimized panel design to meet automated equipment requirements based on EAU increased the master panel utilization from 52% to 72% yielding 20% more panels than the existing design and providing high throughput and lower cost per unit.

### Value Engineering Services Implemented

<table>
<thead>
<tr>
<th>Service Implemented</th>
<th>Cost Savings</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB Panel Design</td>
<td>$20K</td>
</tr>
</tbody>
</table>

## PCB Material Specification

### Project B

**Scope of the Project**

Relax Tg constraints for 10 layer board and realize savings by switch from S1000-2 (Tg 170) to IT158 (Tg 150) with existing supplier.

### Value Engineering Services Implemented

<table>
<thead>
<tr>
<th>Service Implemented</th>
<th>Cost Savings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design for Fabrication</td>
<td>$34K</td>
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</table>
Design for Testability (DFT)

- Post Routing release enables a physical view of the PCB and actual test points, size and location.
- Physically assigned probe access are analyzed by assigning test point and generating nail rules, keep outs to the design
- Component level coverage for Placement, Functionality, Solderability and Value are provided.
Test Strategy Overview

- **Electrical Testing (Value/Polarity)**
  - Typically involve opens, shorts, impedance and net verification. Powered tests are available to provide some additional coverage options.
  - Strategies include Manufacturing Defect Analyzer (MDA) Flying Probe,

- **Structural Testing (Placement/Polarity)**
  - Typically detects presence, absence, orientation/polarity and solder joint integrity.
  - Strategies include Visual Inspection, X-Ray (2D or 3D) and Automated Optical Inspection (AOI)

- **Functional Testing (Functionality)**
  - Typically involve expected input and output simulation of the end application and exercising of core circuitry to validate final functionality
  - Strategies include In-Circuit Test (ICT) and Functional Test (FT)

- **Reliability Testing (Validation)**
  - Typically involve cycling power / temperature over a statistically determined period to identify pre-mature electrical or structural failure that may effect long term reliability
  - Strategies include Run-in, Burn-in and Environmental Stress Screening (ESS)
Test Strategy Analysis

Test Strategy Analysis provides an overview of current coverage proposed test strategy, expected yield assumptions, coverage gaps and expected RMA.

- **Recommend Test Strategy for optimum coverage and efficiency**

- **Generate Return on Investment based on EAU and lifecycle to design/optimize Test Plan.**

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**Test Strategy ROI Summary**

<table>
<thead>
<tr>
<th>Process</th>
<th>Expected ROI</th>
<th>Expected Yield</th>
<th>Expected Yields</th>
<th>Expected ITYield</th>
<th>Expected Functional Yield</th>
<th>Expected Coverage</th>
<th>Expected NRE</th>
<th>ROI (Yr)</th>
<th>Cost of Quality</th>
<th>Savings</th>
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**Notes:**
1. All Key parameters for quantifying costs is the expense involved in processing field returns. This figure has been estimated at $17.09 per card but should ideally should be set by the customer.
## Test Strategy Recommendation

### Scope of the Project

Review existing test strategy and coverage to determine optimal test strategy to provide highest first pass yield, lowest coverage gaps, RMA and overall cost of quality.

### Value Engineering Services Implemented

<table>
<thead>
<tr>
<th>Service</th>
<th>Potential Savings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design for Test – Recommend AOI and ICT (FCT only required if full analog frequency testing required) over existing AOI and 5DX testing (no electrical). Reduce coverage gaps from 0.24% to 0.04% and expected RMA from 11.38% to 3.94%. ROI 0.20 years.</td>
<td>$89K - $18K = $61K</td>
</tr>
<tr>
<td>ICT Development – Quote includes all aspects of ICT development, including future maintenance and production support.</td>
<td></td>
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</tbody>
</table>
Prototype

- Quick Turn Prototyping
- Distribution Procurement
- Local Suppliers (may or may not be same suppliers as production)
- Usually structural and/or fixtureless electrical testing
- Proof of Concept or early Alpha/Beta builds
- Initial FMEA and Control Plan Development

**Who should be engaged?**

- Critical Component Suppliers
- Manufacturer
- Test Engineering
- Quality

**DfX Review**

- **Design for Manufacturability (DFM)**
  - Equipment Requirements
  - Tooling Considerations
  - Process Considerations
  - Labor Requirements
Design for Manufacturing (DFM)

- DFM incorporate supplier specific equipment requirements, specific manufacturer process requirements are applied to develop the process and ultimately the Control Plan to effectively address the pFMEA.
Validation

- Design Verification Testing (DVT)
- Highly Accelerated Life Test (HALT)
- Highly Accelerated Stress Screen (HASS)

Who should be engaged?
- Reliability Engineering
- Test Engineering
- Quality

DfX Review
- Design for Reliability (DFR)
  - HASS/HALT Failure Mode Inputs
Validation is intended to exercise the design within and outside their indeed specifications with the objective to test the limits of the design.

Test Plans may include
- Design Verification Test
  - Utilizes relatively low stresses and requires many cycles
- Design Vibration, Drop and Impact
- Design Highly Accelerated Life Test (HALT)
  - Purpose to determine the operating and destructive limits of a design.
  - Verify designs, component selections and manufacturing processes
- Design Highly Accelerated Stress Screen (HASS)
  - Test methods specifically designed on finding defects in products

A traditional DFR “test-in reliability” approach which is valuable to identify “weak links” provides closed loop validation in conjunction with DfX methodology to further improve value.
New Product Introduction

- Final Design Release
- Volume Production Supplier Awards
- Critical Component and Control Plan in Place
- Introduction of Production Tooling/Process
- Master Validation Process Plan
  - IQ, OQ, PQ Development

Who should be engaged?
- Critical Component Suppliers
- Manufacturers/ Procurement
- Test Engineering
- Quality

DfX Review
- **Design for Manufacturability (DFM)**
  - First Article Reports
  - Process Development (pFMEA)
  - Yield and Detractor Analysis
  - Problematic Design Improvements
- **Design for Testability (DFT)**
  - Coverage Gap Strategy
Early Supplier involvement and detailed DFX inputs provide invaluable insight when developing the FMEA and should be mandated across all suppliers where practical.

**Areas reviewed include**

- First Article Routing and Cycle Time
- Automation – Panel Design, Supply Compatibility
- Tooling – Stencils, Pallets, Other
- Process – SMD, Reflow, Wave, Mechanical
- Misc. Process – Conformal Coating, Cabling, System Integration
- Program Parts
- AOI/5DX Testing
- FP/ICT/FT Testing
- Hi-Pot/ESS Testing
- Misc. Testing – Buss out, continuity
- Quality – First Pass Yield, Top 5 detractors
- First Article Sign Off
Production

- Full Production Ramp/ Sustaining
- Stable Process and Test
- Duplication of existing Process/ Test Equipment (Capacity/ Throughput)
- Continuous Improvement
- Value Engineering

Who should be engaged?
- Critical Component Suppliers
- Manufacturers
- Test Engineering
- Process Engineering
- Quality Engineering

DfX Opportunities
- Design for Supply Chain (DFSC)
  - EOL and PCN Management
  - Cost Reduction
- Design for Testability (DFT)
  - Test Improvements/ Reductions
- Design for Manufacturing (DFM)
  - Process Improvements
Early Supplier Involvement Benefits

- Early design interface and collaboration among designers, buyers, and suppliers throughout the product development cycle significantly improve the ability to impact the design.

- Identifying risks early enables customers to better manage their design.

- Resulting overall lower project costs and higher **VALUE Products**
THANK YOU
### DFX Engagement Case Study

<table>
<thead>
<tr>
<th><strong>Examples</strong></th>
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<td><strong>Design for Supply Chain (DFSC)</strong></td>
</tr>
<tr>
<td>Perform BOM and Lifecycle Analysis to identify EOL and discontinued early in the procurement cycle.</td>
</tr>
<tr>
<td>Supported last time buy and provided FFF alternates to support design</td>
</tr>
<tr>
<td>Performed AML Expansion to provide cost savings and supply chain flexibility</td>
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</tbody>
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| **Design for Assembly (DFA)** |
| Performed Stack up Tolerance and Interference Analysis to identify manufacturing and assembly issues. |
| Performed Valor virtual part and DFM analysis of all printed circuit boards to identify assembly and design related issues. |

| **Design for Manufacturability (DFM)** |
| Incorporated early supplier involvement and DFM with key Metal, PCB and Plastic Suppliers |
| Established manufacturing tolerances and capabilities into tolerance and stack up to provide critical dimensions to ensure function of final unit. |

| **Design for Testability** |
| Performed Board and System level schematic review |
| Utilizing Test Expert performed Nodal access and Coverage Reporting |
| Provided Test Strategy Analysis and Functional Recommendation |

| **Design and Development** |
| Combined Solidworks models and perform Analysis |
| Re-layout flex cable to optimize via positions and decrease connector footprint |
| Re-layout sensor board to move traces and address shorting issues |
| Develop custom automated lens focusing and system level test fixture. |