Design for Excellence (DFX)

Driving Product Optimization Through Early Stage Supplier Engagement

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smtc

manufacturing partner® to innovators

SMTC Corporation

- Established in 1985
- Over 600,000 square feet of manufacturing capability
- Facilities that covers a large global footprint
- More than 40 manufacturing and assembly lines
- Approximately 1,300 employees
- Listed on NASDAQ since 2000 (SMTX)
- Frost & Sullivan Awards Winners – Growth Leadership and Product Quality Leadership Awards

Our Vision

To simplify the lives of our customers by delivering extraordinary Customer Service, Responsiveness, Quality, Technology Solutions and Value, fueling their Success and Our growth

Our Values

- Solution Oriented
- Collaborative Partner
- Professional integrity
- Proactive
- Innovative
- Dependable

Medical Device Markets

Specialists in the Design and Manufacture of Complex Class I and II Medical Devices

We design and manufacture class I and II medical devices that require a mix of highly specialized technologies including:

- Diagnostic devices
- Imaging equipment
- laboratory equipment
- Patient Monitoring systems
- Infusion Pumps
- Dispensing Systems
- Consumer Wellness Products.





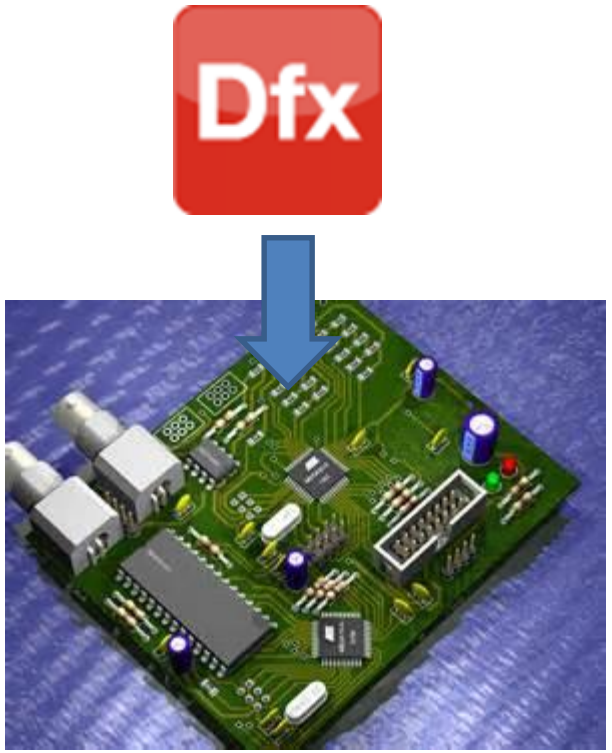
DFX Product Optimization

- What is DFX?
- DFX Benefits
- Product Value Equation
- Ability to Impact Product Value
- Early Supplier Involvement (ESI)
- Product Development
  - dFMEA
  - Design for Reliability (DFR)
  - Design for Supply Chain (DFSC)
- High Level Design
  - Design for Testability (DFT)
- Physical Design
  - PCB Design Engagement
  - Design for Assembly (DFA)
  - Design for Reliability (DFR)
  - Design for Fabrication (DFF)
  - Design for Testability (DFT)
- Prototype
  - Design for Manufacturing (DFM)
- Validation
  - Design for Reliability (DFR)
- New Product Introduction
  - FMEA and Control Plan
- Production
- ESI Benefits

What is DfX?

- **DFX** or **Design for eXcellence** is the application of Rules, Guidelines and Methodologies during the Product Development with the purpose of impacting it's **Value** while meeting the Product Design Requirements.
- The **x** in Df**x** represents an aspect of the product value to be targeted; these may include (*but not limited to*)

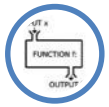
- **Design for Supply Chain (DFSC)**
  - Process of ensuring material sourcing, supply, compliancy and lifecycle requirements are met during design stage.
- **Design for Reliability (DFR)**
  - Process for ensuring reliability of a product or system during the design stage ***before*** physical prototype
- **Design for Fabrication (DFF)**
  - Process of ensuring the manufacturability of the PCB fabrication design and related cost drivers are met.
- **Design for Assembly (DFA)**
  - Process of ensuring the assembly of the PCB design and physical layout rules are met prior to prototype
- **Design for Manufacturability (DFM)**
  - Process of ensuring the manufacturability of a component or complete assembly to met supplier's capability.
- **Design for Test (DFT)**
  - Process of analyzing test access, coverage and schematics are designed for test

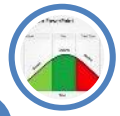


DFX Benefits

- **Product Design for Manufacturability**
  - Improved PCB yield, performance and cost **(DFF)**
  - Improved Assembly yield and reduced labour content **(DFA)**
- **Product Design for Testability**
  - Improved Coverage, Reliability and Final yield, reduced RMA and field failures. **(DFT, DFR)**
  - Reduced development engineering resource commitment, improved time to market
- **Product/ Process Stability and Repeatability**
  - Reduced lead time, improved availability/lifecycle and material costs **(DFSC)**
  - High quality, reliable and robust performance for the life of the product **(DFR)**
- **Capability**
  - Improved Production Stability and Predictability **(DFM)**
- **First Pass Yield and Capacity**
  - Continuous Improvement **(DFM)**

Product Value Equation


Function


Lifetime

Quality


Reliability


Features

PERFORMANCE

Performance can be a function, need, feature or aspect that is deemed critical to the product design.


PCB


Testing

Components


Labor


Design

COST

Cost can include material, labor, test, logistics or any other aspect required to provide the required performance.

VALUE

Ability to Impact Product Value

	Architecture	High Level Design	Physical Design	Prototype	Validation	NPI	Volume
COSTED ACTIVITIES	• Component selection – Major (e.g. Processor) • Hardware / Software partitioning	• Schematic Design • ASIC/FPGA Design • Component Selection	• PCB Layout • DFM • DFT • Component Selection (e.g. passives)	• Quick Turn Prototype • Early DFM/DFT Feedback	• Device level testing • System integration testing • EMC testing • Agency submissions	• Supply chain tweaking	• Continuous process improvement

DFX ENGAGEMENT

- DFR – Design For Reliability
- DFSC – Design For Supply Chain
- DFT – Design For Test
- DFA – Design for Assembly
- DFF – Design for Fabrication
- DFM – Design for Manufacturability

Early Supplier Involvement (ESI)

Common Development Mistakes

1. Lack of Collaboration and Review of Requirements
2. Poor understanding of supplier capabilities/ limitations
3. Customer expectations (reliability, lifetime, use environment) are not incorporated into the new product development

Best Practice

- Early supplier involvement in the product design cycle can provide customers with a product that is more cost effective, increased manufacturability and quality, has higher reliability and longer overall lifecycle.

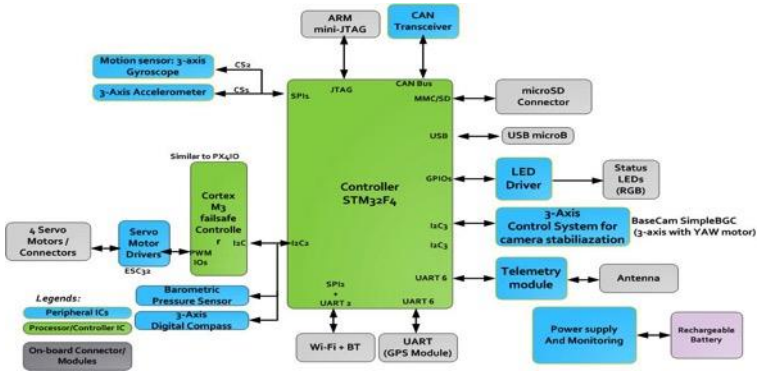
- Design reviews at key stages throughout the design cycle provides critical feedback to address potential issues to ensure a successful new product introduction and high quality, high yielding, reliable and manufacturable product.

Product Development

Architecture | High Level Design | Physical Design | Prototype | Validation | NPI | Volume

Architecture/ Concept Key Activities

- Selection of Critical Components
- Defining Environment Requirements
- Detailed Specifications
- Hardware/ Software Requirements
- Defining Key Functions/ Features



Supplier Engagement

- Major Component Suppliers
- Manufacturer
- Supply Chain/ Procurement

DFX Review

- **Design for Reliability (DFR)**
  - Critical Component Selection
  - Desired Lifetime/ Environment
  - PCB Design Considerations
- **Design for Supply Chain (DFSC)**
  - Predicted Lifecycle and Sourcing
  - Process Compatibility
  - Strategic Supplier Alignment

dFMEA - Design Failure Modes and Effects Analysis

Architecture | High Level Design | Physical Design | Prototype | Validation | NPI | Volume

Impact of Design Decisions

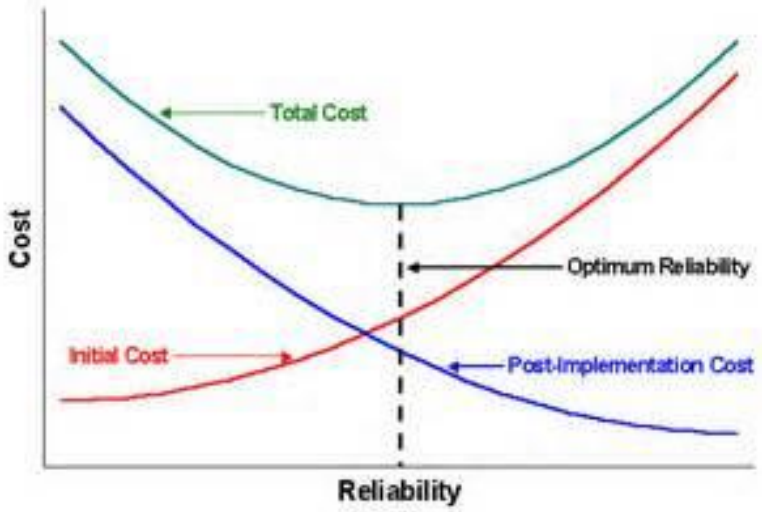
- Although very early in the design cycle, key component suppliers should be providing their component level dFMEA, reliability and design suitability input.
- Reliability and Lifetime decisions made now will be very difficult to change later in the design cycle. A through design review should be made.
- Sourcing and strategic alignment of the supply chain and a predicted EOL should be reviewed.
- Specifying a custom single sourced processor slated to go EOL can limit component availability, time to market and potentially require a complete redesign.

Appendix A

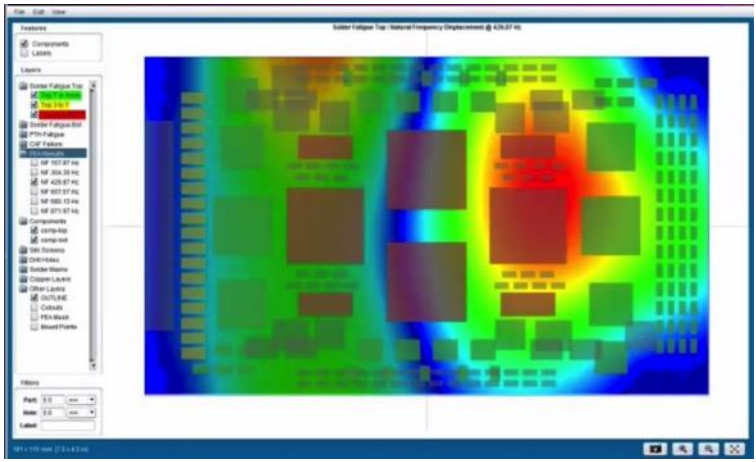
Item	Part	Failure Mode	Local Effect	System Effect	Module Name	Cause	ICT (Y/N)	Mfg Controls	Comments
1.	MSP430 (Link Processor) U1	Pin 4 tied to Pin 5	No Effect assuming both are configured as inputs (internal pull up disabled)	1: None	Link Processor	N/A	Y	5DX, AOI and ICT Functional	
2.		Pin 5 tied to Pin 6	No Effect assuming both pins are inputs	1: None		N/A	Y	5DX, AOI and ICT Functional	
3.		Pin 6 tied to Pin 7	No Effect assuming both pins are inputs	1: None		N/A	Y	5DX, AOI and ICT Functional	
4.		Pin 7 tied to Pin 8	No Effect assuming both pins are inputs	1: None		N/A	Y	5DX, AOI and ICT Functional	
5.		Pin 8 tied to Pin 9	Unintended additional load of 0.25mA on internal reference supply of MSP430. (internal pull up disabled on pin 8) No effect.	1: None		N/A	Y	5DX, AOI and ICT Functional	
6.		Pin 9 tied to Pin 10	ADC internal reference circuit will get damaged in MSP430. Analog voltage monitoring cannot be done by MSP430	115: Communication Module power faults will not be monitored		N/A	Y	5DX, AOI and ICT Functional	
7.		Pin 10 tied to Pin 11	Short circuit protection feature will be triggered in U3. MSP430 will not get Analog power supply.	115: Communication Module power faults will not be monitored		N/A	Y	5DX, AOI and ICT Functional	
8.		Pin 11 tied to Pin 12	Short circuit protection feature will be triggered in U3. MSP430 will not get Analog power supply.	115: Communication Module power faults will not be monitored		N/A	Y	5DX, AOI and ICT Functional	

Design for Reliability (DFR)

DFR is performed early in the design cycle to identify approved manufacturer part numbers which for reasons lifecycle, availability, process compatibility or validity are addressed prior to initial design

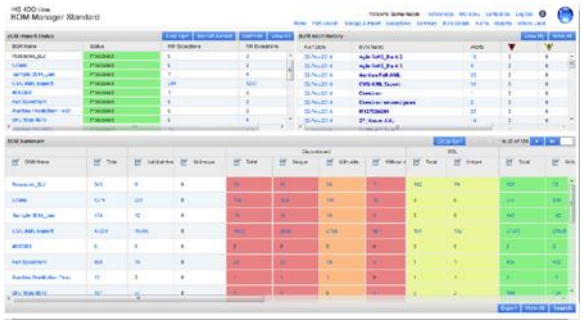


- **Critical Component Considerations**
  - Sensitivity of the circuit to component performance
  - Number of components within the circuit
  - Output from FMEA (Failure Mode Effects Analysis)
  - Historical experience/ Industry data
  - Component technology
  - Tin Whiskers
  - Ceramic Capacitor (Cyclic Voltage)
  - Resistors (High Resistance - SIR)
  - Thick Film Resistors (Sulfide Corrosion)
  - Electrolytic Capacitors
  - Connectors
  - Wear Out – Memory, Relay/Switches/ LED
- **Desired Lifetime**
  - Temperature/ Humidity/ Electrical Load/ Vibration/ Mechanical Stress/ Shock/ Power Cycling
- **PCB Design**
  - Surface Finish - OSP, ENIG, HASL, Immersion Silver
  - Stack up, Laminate (Tg/Td), Blind/Buried Vias, Microfill/ Plating
  - Land Pattern Design, Spacing, Voltage Bias
  - ICT Stress



Design for Supply Chain (DFSC)

DFSC performed early in the design cycle helps to identify selected manufacturer part numbers which for reasons of lifecycle, availability, process compatibility or validity are addressed prior to initial design.



- **BOM Health Check**
  - Review AML data for completeness (orderable) and preferred supply.
  - Ensure MPN match with part description
  - Hazardous Substance Content
  - Manufacturing Process Compatibility
- **BOM Lifecycle Analysis**
  - Form-Fit-Function (FFF) replacement reviews
  - Predicted Lifecycle and YTEOL Forecasts
  - Change Notices and Counterfeit Alerts
- **Value Add**
  - AML Expansion and Preferred supplier selection
  - Supply Chain Optimization
  - EOL and Alternate Qualification
  - Cost Reduction

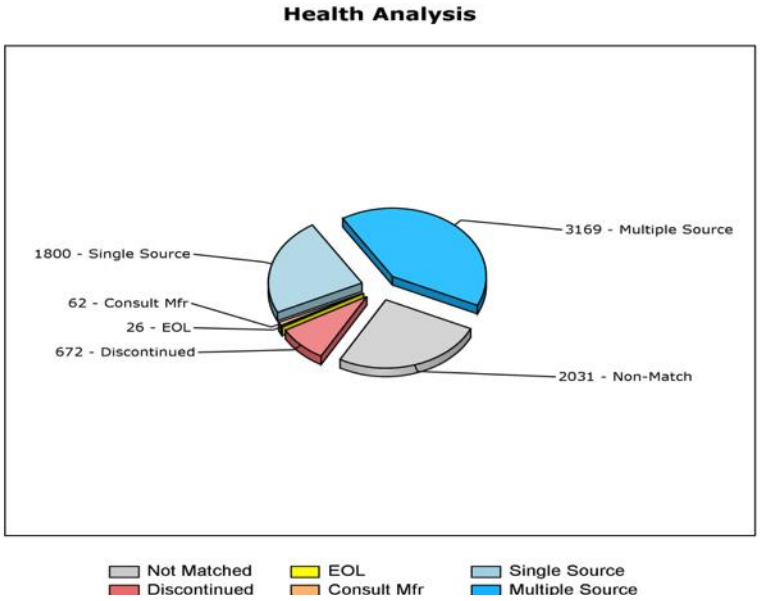
BOM Health Check

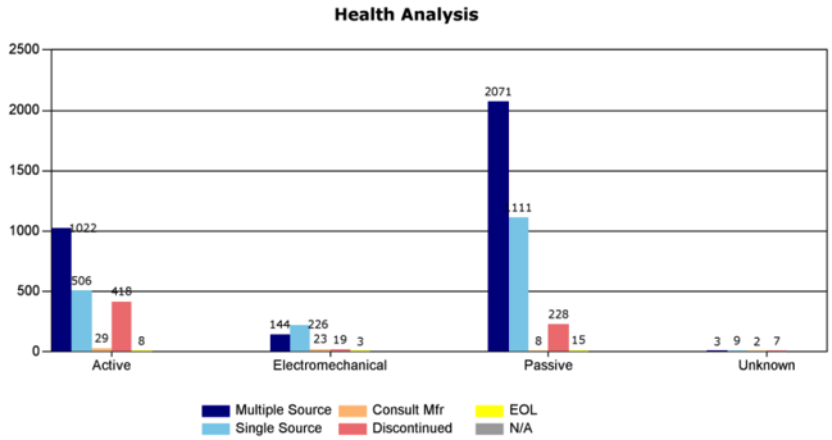
- A BOM Health Analysis services can be performed utilizing leading providers of component information on the global market and economy.
- Advanced reporting tools and prediction services can provide insight on Risk and make informed decisions prior to securing the architecture.

- **Health Analysis**
  - Provides an overall health of the BOM supply chain based on current and predicted lifecycle, available sources and compliancy.
  - **AML**
  - Total AML: 7883
  - Total Active AML: 5093

  - **Risk:**
  - Discontinued w/o Alts: 142
  - Discontinued with Alts: 498
  - EOL: 26
  - Single Sourced 1860
  - RoHS Non-Compliant 87

  - **Calculated Health Score:**
  - **612.6 out of a possible 1000**



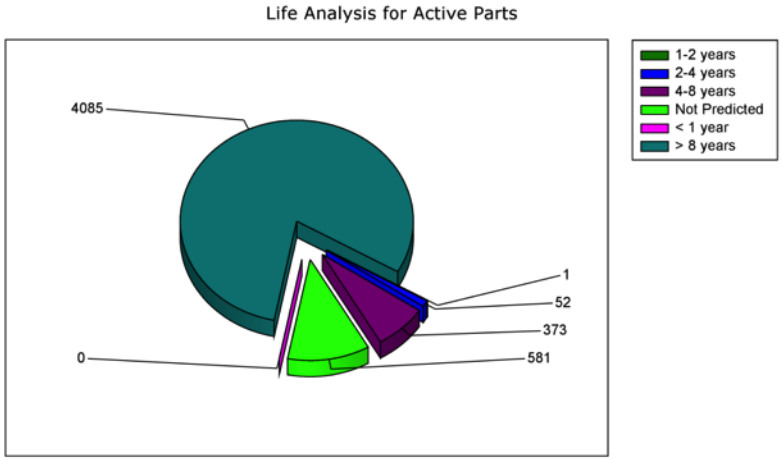


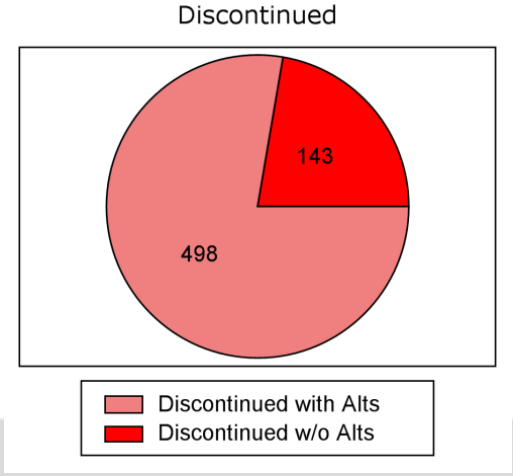
Dfx BOM Analysis

- BOM Analysis provides insight to identifying opportunities and focus to improve supply chain health and AML alternates to address single sourced, EOL/Discontinued, Non-compliant and address material cost drivers.

- **Risk Areas**
- Discontinued AML: 498 w/ alt, 143 w/o alt.
- EOL AML: 26
- Non-compliant: 86
- Single Sourced AML - 1800

- **Value Add**
- Evaluate FFF replacement recommendations or develop strategy to address Discontinued/EOL components.
- Qualify RoHS equivalent orderable part numbers or provide alternates to address compliancy issues
- Align strategic FFF AML Alternates to provide multiple sources to single sourced components.
- Identify opportunities for cost reduction through FFF AML Alternate on existing AML.
- Provide PCN support to proactively notify and address risk.





DFSC Value

AML Expansion	Project A
Scope of the Project	
Targeting cost reduction, 40 parts were identified as FFF alternates to existing approved AML with a potential for 20% reduction in material costs. *Cost avoidance of $38K was identified through alternate sourcing due to obsolesce*	
Value Engineering Services Implemented	***Cost Savings***
▪ Component Engineering	▪ $126K

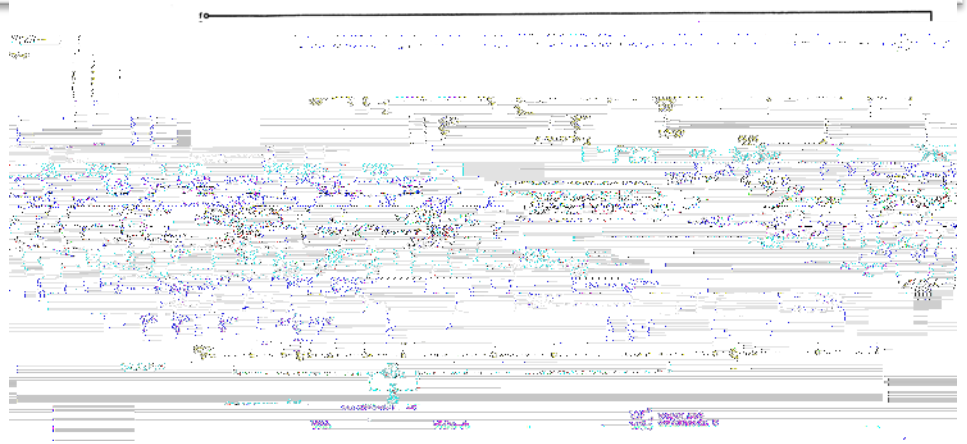
AML Expansion	Project B
Scope of the Project	
Target cost reduction and in-plant store VMI for Power Supply for a potential 8% reduction in cost. *Full functional part evaluation in system and test reports provided to support qualification*	
Value Engineering Services Implemented	***Cost Savings***
▪ Component Engineering	▪ $87K

High Level Design

Architecture	**High Level Design**	Physical Design	Prototype	Validation	NPI	Volume

Hardware Design

- Schematic Design
- ASIC/ FBGA Design
- Cont'd Component Selection
- Hardware/ Software Requirements
- Defining Key Functions/ Features
- Test and Performance Definition



Who should be engaged?

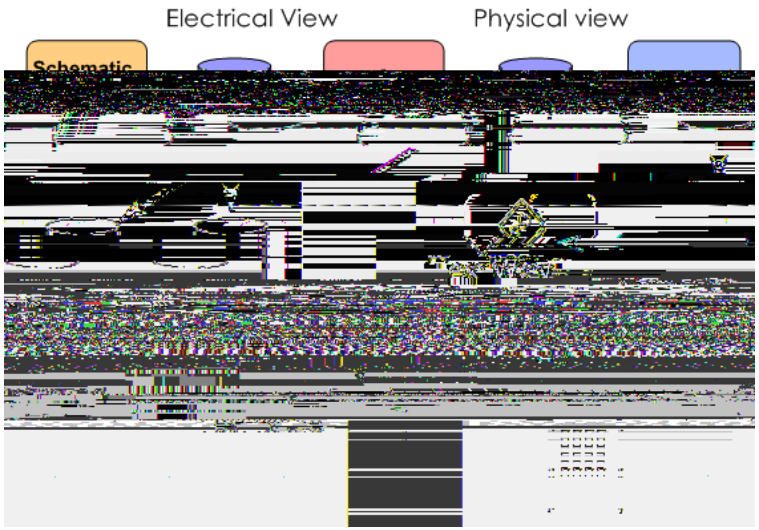
- Supply Chain/ Procurement
- Software Engineers
- Test Development Partners
- Manufacturer

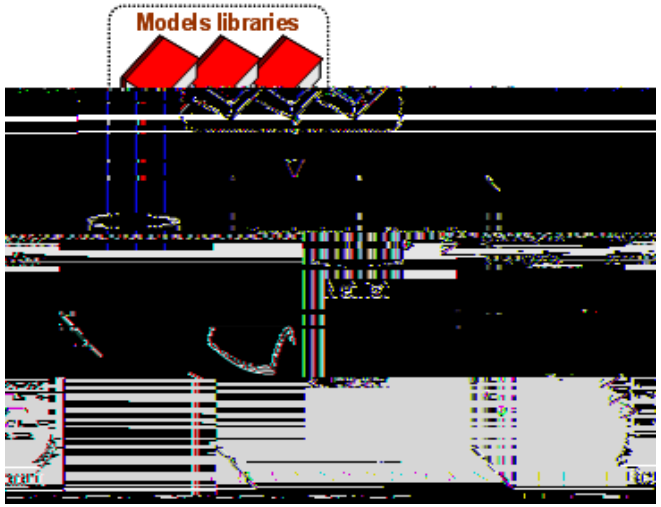
DfX Review

- **Design for Testability**
  - Schematic Review
  - Test Strategy Review
- **Design for Supply Chain (DFSC)**
  - Predicted Lifecycle and Sourcing
  - Process Compatibility
  - Strategic Supplier Alignment

Design for Testability (DFT)

- Early electrical design can be reviewed at the schematic level to identify electrical characteristics of the design that may have a negative impact on in-circuit test coverage or cost.
- Design rule and guidelines checks applied through advanced schematic modelling software can identify costly design errors at high level design.
- Advanced reporting provide comprehensive reports that highlight estimated production yield, test coverage by component, cycle times and validate early dFMEA assumptions.
- Adjustments to the schematic at this high level design to address access and design considerations including JTAG, Boundary Scan and related requirements can significantly reduce the overall cost and complexity of the test strategy.

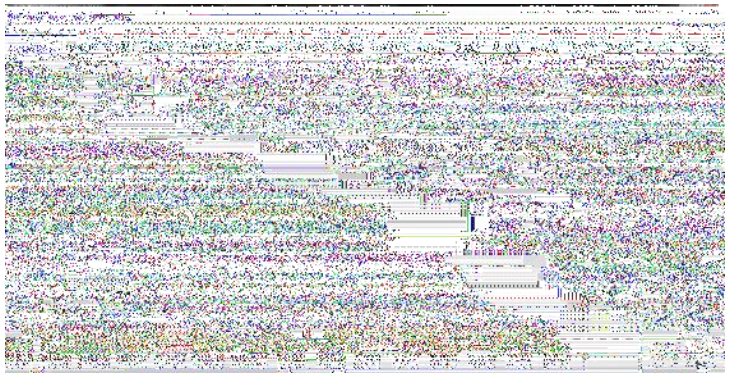




Physical Design

Architecture | High Level Design | **Physical Design** | Prototype | Validation | NPI | Volume

- **PCB Design**
  - PCB Layout and Routing
  - PCB Stackup and Fabrication
  - Final Component Selection
    - Passives
    - Hardware
  - Design File Generation (Gerber, Fab, Placement)



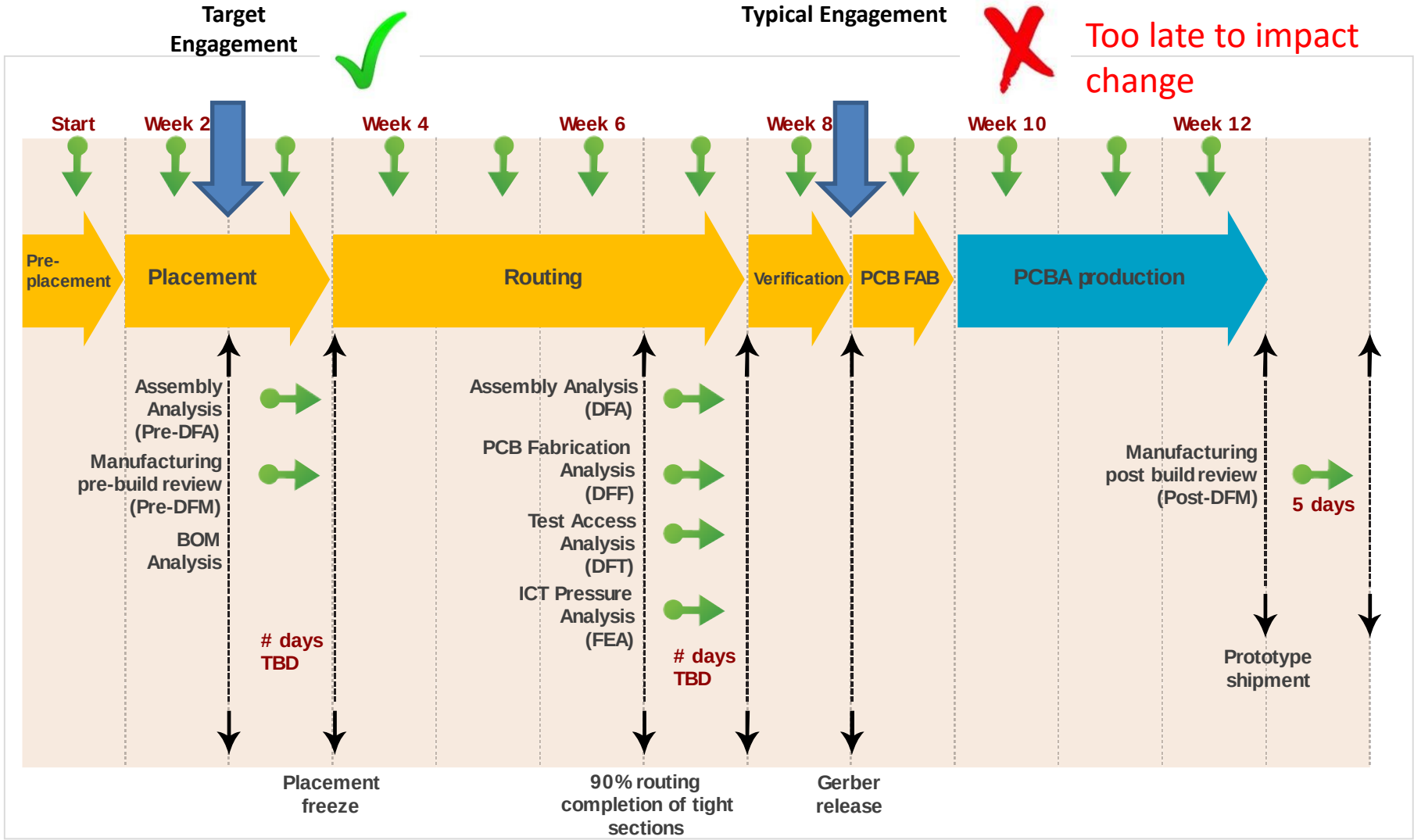
Who should be engaged?

- PCB Designers
- Manufacturers
- PCB Fabrication
- Test Development Partners

DfX Review

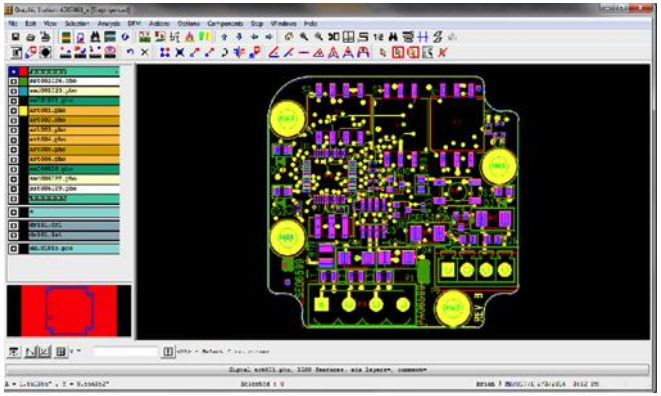
- **Design for Assembly (DFA)**
  - Physical Layout
  - Assembly and Manufacturer
- **Design for Fabrication (DFF)**
  - Stack up and Impedance
  - PCB Fabrication Design Rules
- **Design for Testability (DFT)**
  - Nodal Analysis
  - Test Strategy Development

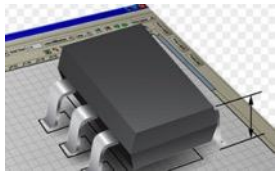
PCB Design Engagement

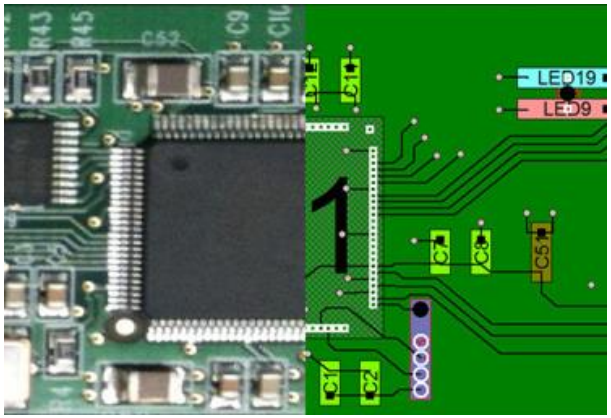


Design for Assembly (DFA)

- Design for Assembly targets opportunities in the physical layout of the assembly to identify areas for improvement and potential areas of concern to drive assembly cost out early in the design cycle.
- Rules and Guidelines are based on your manufacturers capabilities and component requirements.
- Design rules must be configured for your product requirements. i.e. Class 2 or 3, Reliability (Safety critical)
- Advanced software and combined with years of assembly experience. 500+ DFA checks can be performed to provide results on;
  - Component Analysis
  - Pad stack Analysis
  - Pin to Pad Analysis
  - Test Point Analysis
  - Solder Paste Analysis





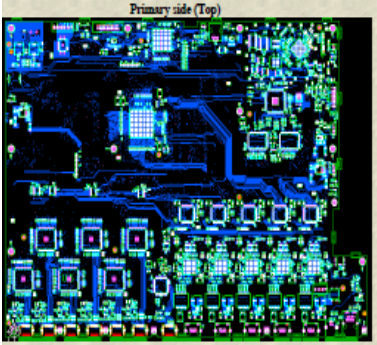


Design for Assembly (DFA)

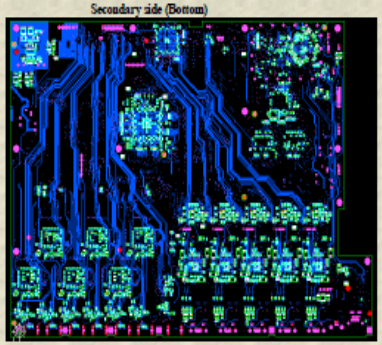
Customer Name:	SMTC Markham - Crestron
Assembly Part Number:	4513218
Assembly Revision:	A
Fab Part Number:	2029611
Fab Revision:	A
BOM Description:	zbom-multilevel-4513218.xls
DFA Engineer:	bhernawan / jlim
Date:	Mon November 12, 2012

PCB Overview; Size: 15.850 x 11.750 "

Primary side (Top)



Secondary side (Bottom)



A. Design Review

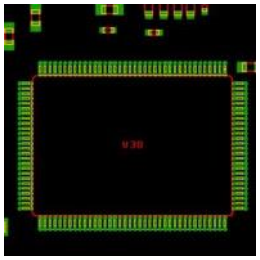
Critical:	Major process/assembly issue
Hot:	Yield improvement suggestion
Warm:	Minor concern
Cool:	No immediate concern
Ignore:	No action required

Id	Title	X-Location (")	Y-location (")	Layers	Refdes	Value-Found (")	Image	All-Dis
1	brdmrg:Short detected	0.165000	7.610000	artwork_photo_01 artwork_photo_01	Short	0.000000		Short circuit detected on board, please verify. Category : Short detected 1. Net +1.8V6A collision with net 1.8V 2. Net +1.0V collision with net 1.0V 3. Net +1.8V3A collision with net $$$13191 4. Net +5VD collision with net $$$4532 5. Net +3.3V collision with net $$$16643 6. Net +5VD collision with net $$$13248 7. Net +24V collision with net +12V_IN Please also check traces under C73.
2	cbk:Trace Under Component C73	3.191250	0.534633	comp_+_top comp_+_top;artwork_photo_01	C73	0.003000		
3	cbk:Testpoint to toeprint P7	3.683000	10.894750	artwork_photo_14 artwork_photo_14;soldermask_photo_14_28;comp_+_top	P7	0.001500		Exposed via is too close to THMT pad on secondary side, it is prone to solder bridge. Please relocate.
3	cbk:Hole in SMD TG1	9.390000	9.230000	artwork_photo_01 artwork_photo_01;comp_+_top;drill	TG1	0.001000		There are vias in pad. Via-in-pad is not recommended as it will cause insufficient solder. If it can't be avoided, it is recommended to fill vias with non-conductive epoxy. Applies to TG1,TP91
4	cbk:Pin Protrusion J7	13.517500	10.725000	comp_+_top comp_+_top	J7	0.000000		Board thickness is 93 mils. Pin is not protruding for this component LEAD STYLE A -01, -L1, -T1 -03, -L3
5	bbmrg:No part in library	11.455000	8.570000	comp_+_top comp_+_top;artwork_photo_01	U140++	0.000000		Some components are excluded from DFM analysis due to no datasheet available on website MARVELL TIGERS ELECTRONICS STAND SQC TECHNOLOGY DELTA FAST BOLT CORPORATION FAST BOLT CORPORATION
6	bbmrg:No part in library	7.845000	0.011488	comp_+_top comp_+_top;artwork_photo_01	J13	0.000000		There are discrepancies on AML. Please refer to "AML discrepancy list.xls" for detail information

Example DFA Output outlining Critical (Major), Hot (Yield improvement), Warm (Minor), Cool (No immediate concern) and Ignore (acceptable)

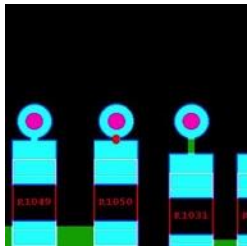
Design for Reliability (DFR)

- **Design for Assembly Reports are an important tool to provide insight into Product failures**
- Utilizing Six Sigma, estimated annualized cost avoidances can be assign to prioritize design change decisions.
- Analysis can be performed to address issues early in the design address potential reliability issues.



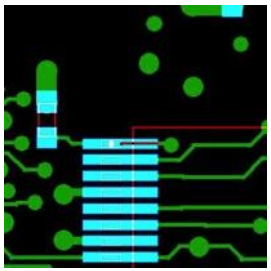
Ref Des U37, U38, distance between pad too close (0.0059”). Prone to solder bridge. Recommend decreasing pad from 13.78 mil to 11 mils.

Quality and Reliability Concern.
2 OFE, 130 Locations – 260 Opportunities
Probability of Occurrence 50%
Expected Yield Detractor 2.5%
Rework Cost $2.80
Potential Failure Cost $4,021.01



Ref R1050, C239, RN96, FB2, etc., masked trace between toe print is too thin, may break and cause insufficient solder. Minimum recommended clearance between exposed via and toeprint is 5mil.

Quality and Reliability Concern.
28 OFE, 14 Location – 392 Opportunities
Probability of Occurrence 40%
Expected Yield Detractor 0.72%
Rework Cost $0.42
Potential Failure Cost $727.50



Ref Des U48, U103, land pattern is not optimal, heel distance is too big. Too much heel may cause solder bridge under component, not visible to visual inspection. Recommended to decrease by 25 mil on heel side.

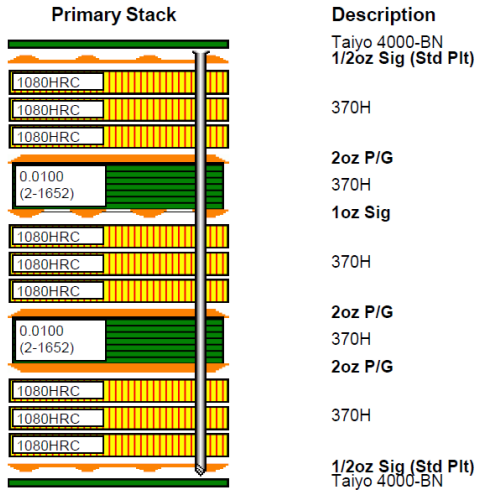
Quality and Reliability Concern.
50 OFE, 2 Location – 100 Opportunities
Probability of Occurrence 50%
Expected Yield Detractor 0.23%
Rework Cost $0.70
Potential Failure Cost $386.63

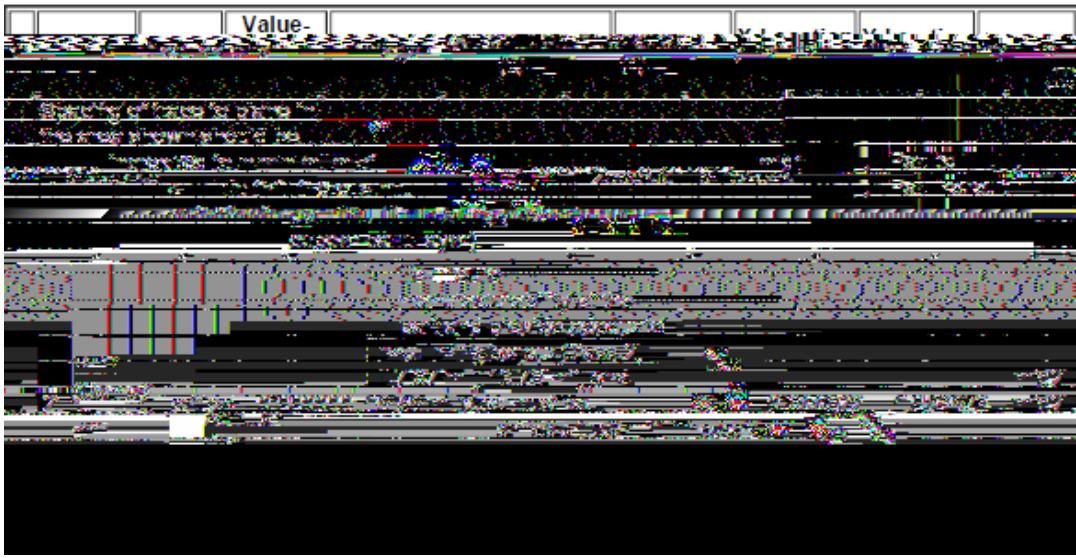
Design for Fabrication (DFF)

- DFF is intended to help review customers' designs with respect to PCB manufacturability as early in the design cycle as possible, where it is easy to make decisions that drive out cost, improve fabrication yields and address concerns before final design is completed.

- Reviews typically include determining workable stackups, including impedance trace widths.

- Most supplier utilize automated DFX tools such as Valor to apply their internal Design Rule Checks (DRC) and will provide comprehensive DFM reports for Design Reviews.





Design for Fabrication (DFF)

- Suppliers will typically provide their DFM guidelines upon request.

VIASYSTEMS

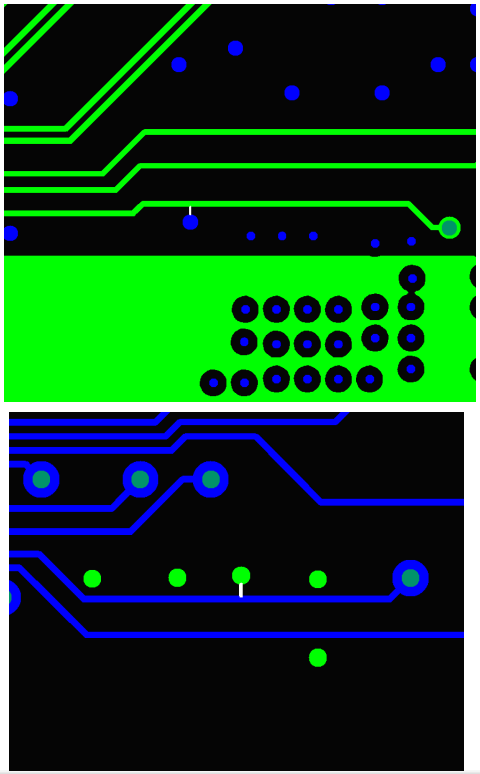
Design For Manufacturability

Customer:	XYZ	stems DCN#:	201305179030
Part #:	ABC	Account Mgr.:	
Revision:		Prepared By:	Reza Bahrami
Cust contact:	Joe Bynd	Date:	5/31/2013

Category	Cust. Data	Edited Manufacturing Data	Predicted Finished Values	Production Preference	Production Minimum (Based on Hoz)	Eng. Approval Required	Verified	
Min. Line Width:								
External Layers	0.0035			0.004	0.0035	<0.0035	☑	
Internal Layers	0.0035			0.004	0.0035	<0.0035	☑	
widths less than .006 wide to minimize galvanic etch during the silver immersion process.								
**Note: If Gold Body boards, the minimum feature spacing is .0045 (Hoz copper)								
Min. Spacing:								
External Layers	0.0034			0.004	0.0035	<0.0035	☑	
Internal Layers	0.0034			0.004	0.00325	<0.00325	☑	
Outer copper wt:	0.50	(Prior to plating)					☑	
Is outer spacing adequate to support specified copper weight?					☑ Yes	☐ No	☑	
Inner copper wt:	0.5/1						☑	
Is inner spacing adequate to support specified copper weight?					☑ Yes	☐ No	☑	
Min.Embedded Trace-To-Gnd Spacing:								
External Layers	0.0148			0.005	**0.005	<0.005	☑	
Internal Layers	0.0148			0.005	0.005	<0.005	☑	
Note: If Gold Body boards, the minimum embedded features spacing is .006 (after etch comp).								
Min. Hole To Cu. Spacing:								
Internal Layers	<0.005			0.010	0.008	<0.008	☑	see note
Min. Annular Ring:								
External Layers	0.004			0.005	0.005	<0.005	☑	

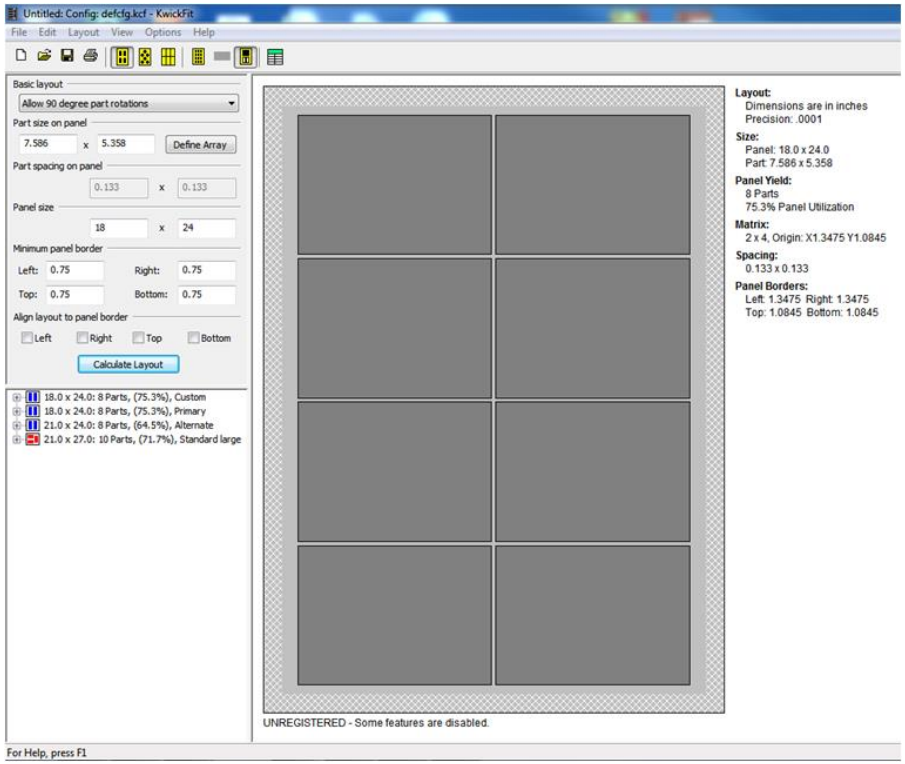
DFM Report | Discrepancies Found | netlist | Sht1 | Sht2 | Sht3 | Sht4 | Sht5 | Sht6 | Stackup

- Incorporating these rules into your native Design Package can help drive value further up the Product Development Cycle



Fabrication Panel Design

- Panel Design is a Primary Cost Driver for PCB
- % Utilization of the Master Panel will typically be the main cost
- Pushing ownership to the fabricator or manufacturer will have it's PROS and CONS.
- It is important that both the fabricator and the manufacturer needs are taken into consideration and collaborative ownership of panel design should be carefully considered.



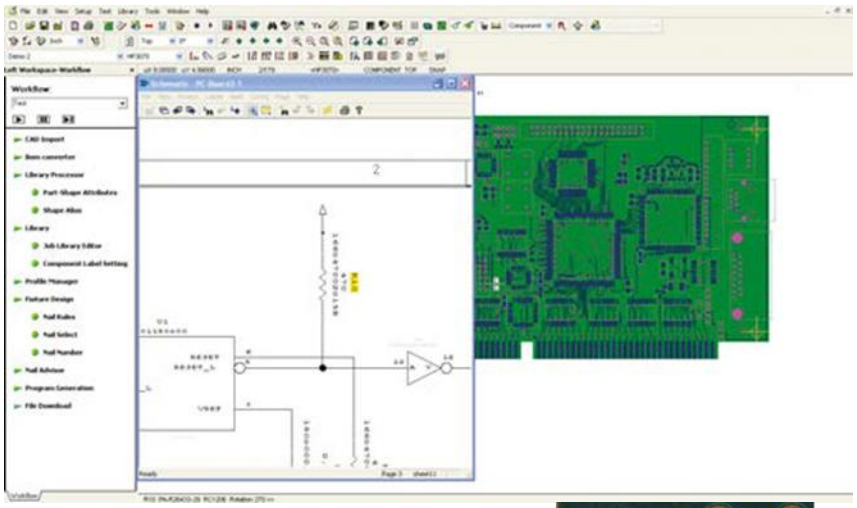
DFF Value

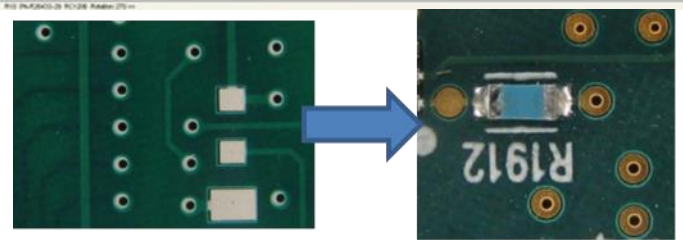
PCB Cost	Project A
Scope of the Project	
Optimized panel design to meet automated equipment requirements based on EAU increased the master panel utilization from 52% to 72% yielding 20% more panels than the existing design and providing high throughput and lower cost per unit.	
Value Engineering Services Implemented	***Cost Savings***
▪ PCB Panel Design	▪ $20K

PCB Material Specification	Project B
Scope of the Project	
Relax Tg constraints for 10 layer board and realize savings by switch from S1000-2 (Tg 170) to IT158 (Tg 150) with existing supplier	
Value Engineering Services Implemented	***Cost Savings***
▪ Design for Fabrication	▪ $34K

Design for Testability (DFT)

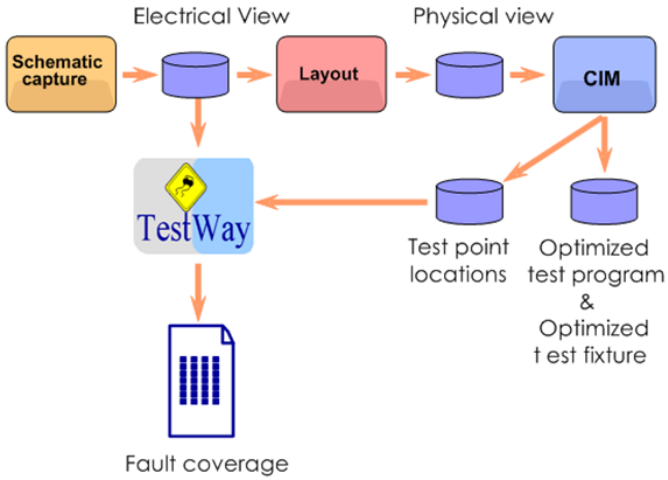
- Post Routing release enables a physical view of the PCB and actual test points, size and location.
- Physically assigned probe access are analyzed by assigning test point and generating nail rules, keep outs to the design
- Component level coverage for Placement, Functionality, Solderability and Value are provided.





PART INFO				PLACEMENT (AOI, ICT, or 5DX)				FUNCTIONALITY (AOI, ICT and 5DX)				VALUE (ICT)				SOLDERABILITY				POLARITY CHECK (AOI, ICT, or 5DX)				% COVERAGE	
REFID	PLACED	TYPE	POLARITY	AOI	ICT	5DX	FINAL	AOI	ICT	5DX	FINAL	AOI	ICT	5DX	FINAL	AOI	ICT	5DX	FINAL	AOI	ICT	5DX	FINAL	OVERALL	FINAL
C1	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C10	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C100	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C1000	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C1001	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C1002	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C1003	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C1004	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C1005	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C1006	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C1007	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C1008	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C1009	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C101	1	C	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	1	1	0	1	1	130%	99%
C1010	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C1011	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C1012	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C1013	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C1014	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%
C1015	1	C	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0	1	1	1	0	1	1	90%	90%

Legend:
1 = Tested
0 = Not Tested
R = Resistor
C = Capacitor
L = Inductors
J = Jumper or
D = Diode
Q = Transistor
U = Integrated
T = Transform
X = Crystal or
RN = Resistor



Dfx Test Strategy Overview

- **Electrical Testing (Value/Polarity)**
  - Typically involve opens, shorts, impedance and net verification. Powered tests are available to provide some additional coverage options.
  - Strategies include Manufacturing Defect Analyzer (MDA) Flying Probe,
- **Structural Testing (Placement/Polarity)**
  - Typically detects presence, absence, orientation/polarity and solder joint integrity.
  - Strategies include Visual Inspection, X-Ray (2D or 3D) and Automated Optical Inspection (AOI)
- **Functional Testing (Functionality)**
  - Typically involve expected input and output simulation of the end application and exercising of core circuitry to validate final functionality
  - Strategies include In-Circuit Test (ICT) and Functional Test (FT)
- **Reliability Testing (Validation)**
  - Typically involve cycling power / temperature over a statistically determined period to identify pre-mature electrical or structural failure that may effect long term reliability
  - Strategies include Run-in, Burn-in and Environmental Stress Screening (ESS)

Test Strategy Analysis

Test Strategy Analysis provides an overview of current coverage proposed test strategy, expected yield assumptions, coverage gaps and expected RMA.

- Recommend Test Strategy for optimum coverage and efficiency
- Generate Return on Investment based on EAU and lifecycle to design/optimize Test Plan.

TEST REPORT FOR ICT,AOI

BOARD NAME / NUMBER	4514473	DATA PROCESSING REPORT	WRK=4514473.htm
COMPONENT	637	COMPONENT TESTED	100.00%
NET	577	NET ACCESS	87.99%
SHORT COVERAGE	100.00%	BOARD SCORE	85.96%

DEVICE TYPE	TOTAL NUMBER (PARTS OR PINS)	Number of well tested	Number of partially tested	Number of not tested
Integrated Circuit	31 Parts (601 Pins)	54.8% (17)	45.2% (14)	0.0% (0)
Transistor	19 Parts	0.0% (0)	100.0% (19)	0.0% (0)
Diode	55 Parts	90.9% (50)	9.1% (5)	0.0% (0)
Capacitor	132 Parts	43.9% (58)	56.1% (74)	0.0% (0)
Resistor	295 Parts	100.0% (295)	0.0% (0)	0.0% (0)
Fuse	16 Parts	100.0% (16)	0.0% (0)	0.0% (0)
Strap	33 Parts	100.0% (33)	0.0% (0)	0.0% (0)
Connector	5 Parts (43 Pins)	40.0% (2)	60.0% (3)	0.0% (0)
Not Mounted	51 Parts			
Total	586 Parts (51 ignored)	80.4% (471)	19.6% (115)	0.0% (0)

smtc
defining manufacturing solutions

TEST STRATEGY ROI SUMMARY

Customer :
Product p/n :
Quote:
EAU:

Test Option ROI

		Expected Final Yield	Expected AOI Yield	Expected SDX Yield	Expected FP Yield	Expected ICT Yield	Expected Functional Yield	Escapes (Coverage Gaps)	Expected RMA	NRE	ROI (yrs)	Cost of Quality	Savings
Quoted Process ->	V	99.91%						0.03%	0.12%	$0.00	0.00	$120.56	$0.00
	V	99.91%						0.03%	0.12%	$ -	0.00	$120.56	$ -
	A	99.94%	99.94%					0.00%	0.07%	$ 300.00	5.86	$69.34	$ 51.22
	X	99.92%		99.95%				0.00%	0.08%	$ 750.00	20.35	$83.70	$ 36.86
	W	99.95%			99.92%			0.00%	0.05%	$ 1,200.00	17.04	$50.14	$ 70.42
	I	99.99%				99.88%		0.00%	0.01%	$ 14,300.00	134.04	$13.88	$ 106.68
	F	99.99%					99.88%	0.00%	0.01%	$ 9,000.00	82.09	$10.92	$ 109.64
	A X	99.94%	99.93%	100.00%				0.00%	0.06%	$ 1,050.00	19.86	$67.69	$ 52.87
	A W	99.97%	99.90%		100.00%			0.00%	0.03%	$ 1,500.00	17.82	$36.40	$ 84.16
	A I	99.99%	99.88%			100.00%		0.00%	0.01%	$ 14,600.00	133.51	$11.20	$ 109.36
	A F	100.00%	99.88%				100.00%	0.00%	0.00%	$ 9,300.00	82.84	$8.29	$ 112.27
	X W	99.97%		99.90%	100.00%			0.00%	0.03%	$ 1,950.00	23.30	$36.86	$ 83.70
	X I	99.99%		99.88%		100.00%		0.00%	0.01%	$ 15,050.00	137.33	$10.97	$ 109.59
	X F	99.99%		99.88%			100.00%	0.00%	0.01%	$ 9,750.00	88.15	$9.95	$ 110.61
	I F	100.00%				99.88%	100.00%	0.00%	0.01%	$ 23,300.00	209.97	$9.59	$ 110.97
	W F	100.00%			99.88%		100.00%	0.00%	0.01%	$ 10,200.00	92.50	$10.29	$ 110.27
	A X W	99.97%	99.90%	100.00%	100.00%			0.00%	0.03%	$ 2,250.00	25.82	$33.43	$ 87.13
	A X I	99.99%	99.88%	100.00%		100.00%		0.00%	0.01%	$ 15,350.00	139.19	$10.28	$ 110.28
	A X F	100.00%	99.88%	100.00%			100.00%	0.00%	0.00%	$ 10,050.00	89.28	$8.00	$ 112.56
	A W F	100.00%	99.87%		100.00%		100.00%	0.00%	0.00%	$ 10,500.00	91.39	$5.67	$ 114.89
	A I F	100.00%	99.87%			100.00%	100.00%	0.00%	0.00%	$ 23,600.00	204.27	$5.03	$ 115.53
	X I F	100.00%		99.88%		100.00%	100.00%	0.00%	0.00%	$ 24,050.00	211.62	$6.92	$ 113.64
	X W F	100.00%		99.88%	100.00%		100.00%	0.00%	0.00%	$ 10,950.00	96.84	$7.49	$ 113.07
	A X I F	100.00%	99.87%	100.00%		100.00%	100.00%	0.00%	0.00%	$ 24,350.00	210.08	$4.65	$ 115.91
	A X W F	100.00%	99.88%	100.00%	100.00%		100.00%	0.00%	0.00%	$ 11,250.00	98.06	$5.83	$ 114.73

V = VM
A = AOI
X = XRAY
W = Flying Probe
I = ICT
F = Funct Test

Recommended test strategy

Recommendation	Expect Final Yield	AOI Yield	SDX Yield	FP Yield	ICT Yield	Functional Yield	Escapes (Coverage Gaps)	Actual RMA	NRE	ROI	Cost of Quality	Savings
A	99.94%	99.94%					0.00%	0.07%	$300.00	5.86	$69.34	$51.22

Notes:
1. A key parameter for quantifying costs is the expense involved in processing field returns. This figure has been estimated at $17.09 per card but should ideally should be set by the customer.

DFT Value

Test Strategy Recommendation	Project A
Scope of the Project	
Review existing test strategy and coverage to determine optimal test strategy to provide highest first pass yield, lowest coverage gaps, RMA and overall cost of quality.	
Value Engineering Services Implemented	***Potential Savings***
▪ Design for Test– Recommend AOI and ICT (FCT only required if full analog frequency testing required) over existing AOI and 5DX testing (no electrical). Reduce coverage gaps from 0.24% to 0.04% and expected RMA from 11.38% to 3.94%. ROI 0.20 years. ▪ ICT Development – Quote includes all aspects of ICT development, including future maintenance and production support.	▪ $89K - $18K = $61K

Prototype

Architecture | High Level Design | Physical Design | **Prototype** | Validation | NPI | Volume

- Quick Turn Prototyping
- Distribution Procurement
- Local Suppliers (may or may not be same suppliers as production)
- Usually structural and/or fixtureless electrical testing
- Proof of Concept or early Alpha/Beta builds
- Initial FMEA and Control Plan Development

Who should be engaged?

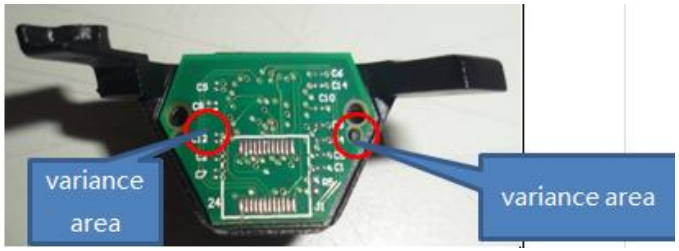
- Critical Component Suppliers
- Manufacturer
- Test Engineering
- Quality

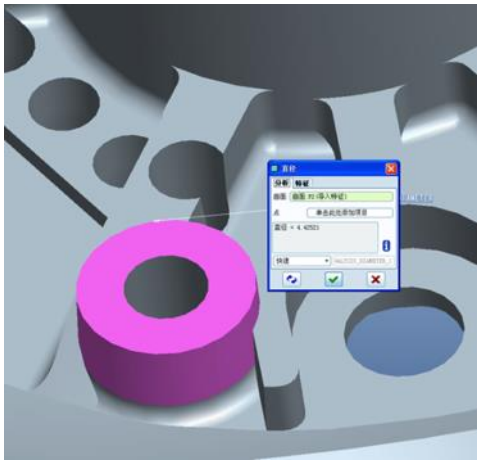
DfX Review

- **Design for Manufacturability (DFM)**
  - Equipment Requirements
  - Tooling Considerations
  - Process Considerations
  - Labor Requirements

Design for Manufacturing (DFM)

- DFM incorporate supplier specific equipment requirements, specific manufacturer process requirements are applied to develop the process and ultimately the Control Plan to effectively address the pFMEA.





CONTROL PLAN

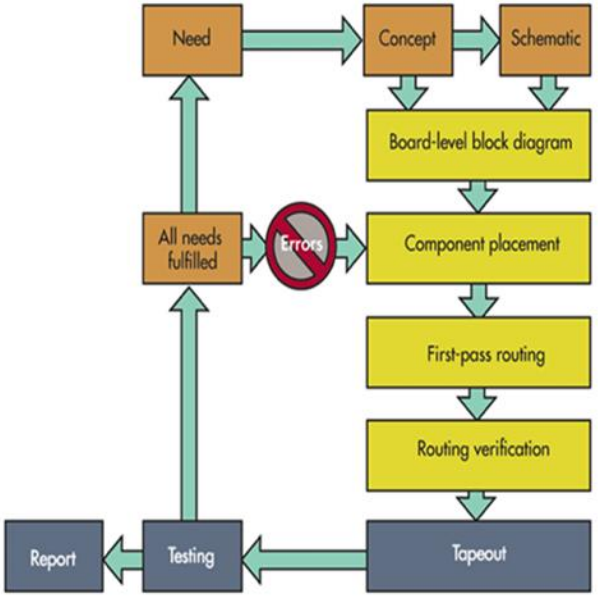
Code :
Rev. :
Location : Quality
Retention :

X	Prototype		Pre-launch		Production	Key Contact/Phone			Date (Orig.)			Date (Rev.)		
Control Plan Number														
Part Number/Latest Change Level						Core Team			Customer Engineering Approval/Date (If Req'd.)					
XXXXXXX						XXXXXXX			N/A					
Part Name/Description						Supplier/Plant Approval/Date			Customer Quality Approval/Date (If Req'd.)					
XXXXXXXX						XXXXXXX								
Supplier/Plant			Supplier Code			Other Approval/Date (If Req'd.)			Other Approval/Date (If Req'd.)					
SMTC Corp. (Markham)			N/A			N/A			N/A					
Process	Process Name/ Operation Description	Machine, Device, Jig. Tools For Mfg.	Characteristics			Special Char. Class	Methods					Control Method	Reaction Plan	
			No.	Product	Process		Product/Process Specification/ Tolerance	Evaluation/ Measurement Technique	Sample					
									Size		Freq.			
Material Control	Receiving Inspection	NA	1	SIT ASSEMBLY	Receiving Inspection	N/A	SMTC WI-0155 WI-0331, receiving inspection workinstructions, WI-0125 Receiving inspection Database	Visual Inspection, AVL, PO	According to sampling plan WI-0155		100%	RI database, AVL	* Notify Supervisor/QE * Hold produced units * Rework defects * Return shipped product. * NCM	
	CAROUSEL & PICK KIT	Carousel	2	SIT ASSEMBLY	Pick Kit	N/A	WI-0165 Handling & SOP-0035 General procedures for storage and handling	Visual Inspection, AVL, Scan the carrier against the individual WO	100% Visual Inspection		100%	Carousel Software , Pick List, WO		
Manufacturing Assembly (Final Integration)	Mechanical Assembly	Torque Driver, Mechanical Fixture, CIM Terminal, Scanner	3	SIT ASSEMBLY	Mechanical Assembly	N/A	According to the specifications of torque in the process, Customer Specifications	Visual check daily calibration label	100% Visual Inspection		100%	Product Binder / BOM / Drawing	Notify Supervisor / QE / PE. * Hold produced units * Return shipped product	
			4				According to Manufacturing	Visual				Product Binder /	Notify Supervisor / QE / PE. * Hold produced	

Validation

Architecture | High Level Design | Physical Design | Prototype | **Validation** | NPI | Volume

- Design Verification Testing (DVT)
- Highly Accelerated Life Test (HALT)
- Highly Accelerated Stress Screen (HASS)



Who should be engaged?

- Reliability Engineering
- Test Engineering
- Quality

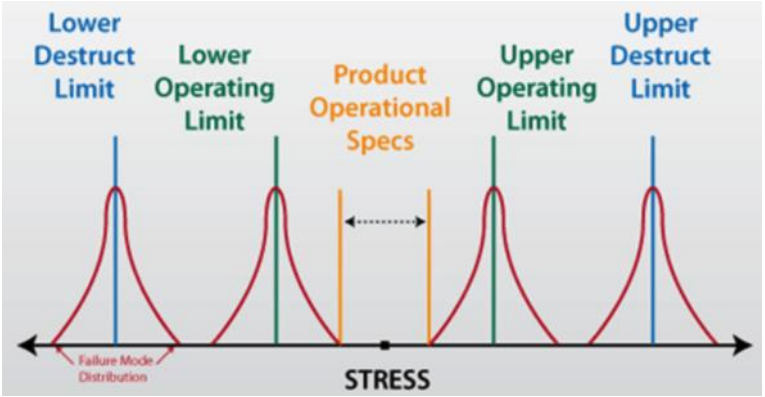
DfX Review

- **Design for Reliability (DFR)**
  - HASS/HALT Failure Mode Inputs

Design for Reliability (DFR)

- Validation is intended to exercise the design within and outside their indeed specifications with the objective to test the limits of the design.

- Test Plans may include
  - Design Verification Test
    - Utilizes relatively low stresses and requires many cycles
  - Design Vibration, Drop and Impact
  - Design Highly Accelerated Life Test (HALT)
    - Purpose to determine the operating and destructive limits of a design.
    - Verify designs, component selections and manufacturing processes
  - Design Highly Accelerated Stress Screen (HASS)
    - Test methods specifically designed on finding defects in products



A traditional DFR “test-in reliability” approach which is valuable to identify “weak links” provides closed loop validation in conjunction with DfX methodology to further improve value.

New Product Introduction

Architecture | High Level Design | Physical Design | Prototype | Validation | **NPI** | Volume

- Final Design Release
- Volume Production Supplier Awards
- Critical Component and Control Plan in Place
- Introduction of Production Tooling/Process
- Master Validation Process Plan
  - IQ, OQ, PQ Development

Who should be engaged?

- Critical Component Suppliers
- Manufacturers/ Procurement
- Test Engineering
- Quality

DfX Review

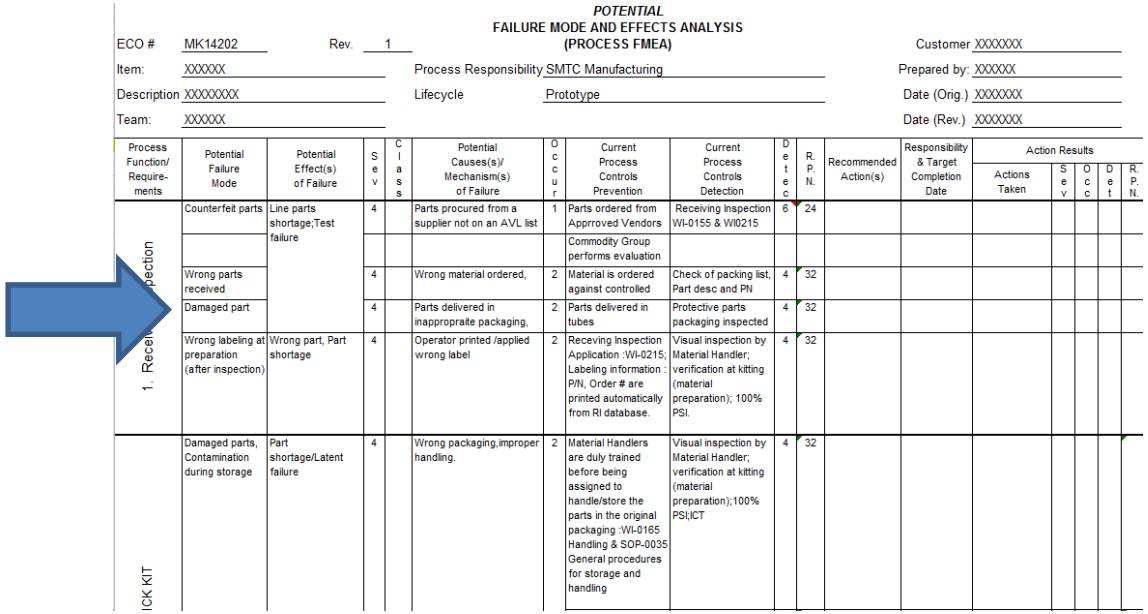
- **Design for Manufacturability (DFM)**
  - First Article Reports
  - Process Development (pFMEA)
  - Yield and Detractor Analysis
  - Problematic Design Improvements
- **Design for Testability (DFT)**
  - Coverage Gap Strategy

pFMEA - Process Failure Modes and Effects Analysis

- Early Supplier involvement and detailed DFX inputs provide invaluable insight when developing the FMEA and should be mandated across all suppliers where practical.

Areas reviewed include

- First Article Routing and Cycle Time
- Automation – Panel Design, Supply Compatibility
- Tooling – Stencils, Pallets, Other
- Process – SMD, Reflow, Wave, Mechanical
- Misc. Process – Conformal Coating, Cabling, System Integration
- Program Parts
- AOI/5DX Testing
- FP/ICT/FT Testing
- Hi-Pot/ESS Testing
- Misc. Testing – Buss out, continuity
- Quality – First Pass Yield, Top 5 detractors
- First Article Sign Off



POTENTIAL
FAILURE MODE AND EFFECTS ANALYSIS
(PROCESS FMEA)

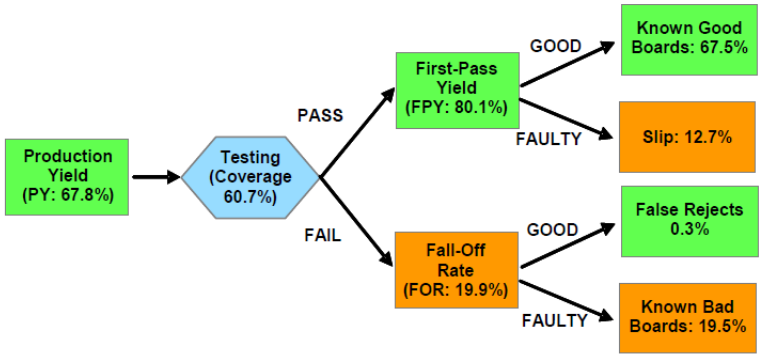
ECO # MK14202 Rev. 1 Customer XXXXXX
Item: XXXXXX Process Responsibility SMTC Manufacturing Prepared by: XXXXXX
Description XXXXXXX Lifecycle Prototype Date (Orig.) XXXXXX
Team: XXXXXX Date (Rev.) XXXXXX

Process Function/ Require-ments	Potential Failure Mode	Potential Effect(s) of Failure	Sev	Class	Potential Cause(s)/ Mechanism(s) of Failure	Occur	Current Process Controls Prevention	Current Process Controls Detection	Det	R.P.N.	Recommended Action(s)	Responsibility & Target Completion Date	Action Results: Actions Taken	Sev	Occ	Det	R.P.N.
1. Receiving Inspection	Counterfeit parts	Line parts shortage;Test failure	4		Parts procured from a supplier not on an AVL list	1	Parts ordered from Apprroved Vendors	Receiving Inspection WI-0155 & WI0215	6	24							
							Commodity Group performs evaluation										
	Wrong parts received		4		Wrong material ordered,	2	Material is ordered against controlled	Check of packing list, Part desc and PN	4	32							
	Damaged part		4		Parts delivered in inappropraite packaging,	2	Parts delivered in tubes	Protective parts packaging inspected	4	32							
	Wrong labeling at preparation (after inspection)	Wrong part, Part shortage	4		Operator printed /applied wrong label	2	Receving Inspection Application :WI-0215; Labeling information : P/N, Order # are printed automatically from RI database.	Visual inspection by Material Handler; verification at kitting (material preparation); 100% PSI.	4	32							
ICK KIT	Damaged parts, Contamination during storage	Part shortage/Latent failure	4		Wrong packaging,improper handling.	2	Material Handlers are duly trained before being assigned to handle/store the parts in the original packaging :WI-0165 Handling & SOP-0035 General procedures for storage and handling	Visual inspection by Material Handler; verification at kitting (material preparation);100% PSI;ICT	4	32							

Production

Architecture | High Level Design | Physical Design | Prototype | Validation | NPI | **Volume**

- Full Production Ramp/ Sustaining
- Stable Process and Test
- Duplication of existing Process/ Test Equipment (Capacity/ Throughput)
- Continuous Improvement
- Value Engineering



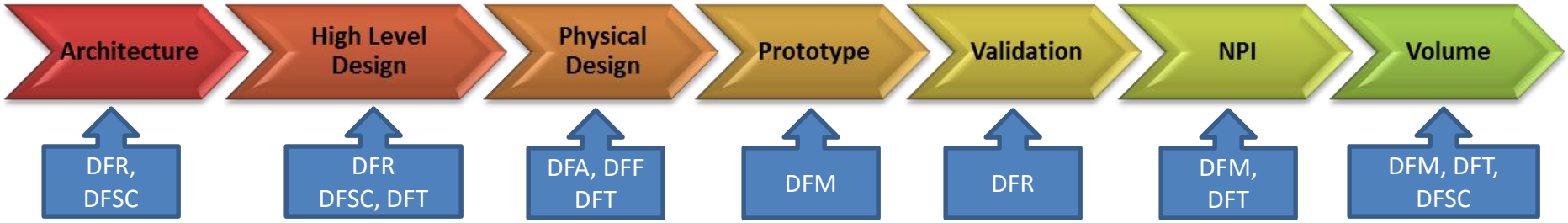
Who should be engaged?

- Critical Component Suppliers
- Manufacturers
- Test Engineering
- Process Engineering
- Quality Engineering

DfX Opportunities

- **Design for Supply Chain (DFSC)**
  - EOL and PCN Management
  - Cost Reduction
- **Design for Testability (DFT)**
  - Test Improvements/ Reductions
- **Design for Manufacturing (DFM)**
  - Process Improvements

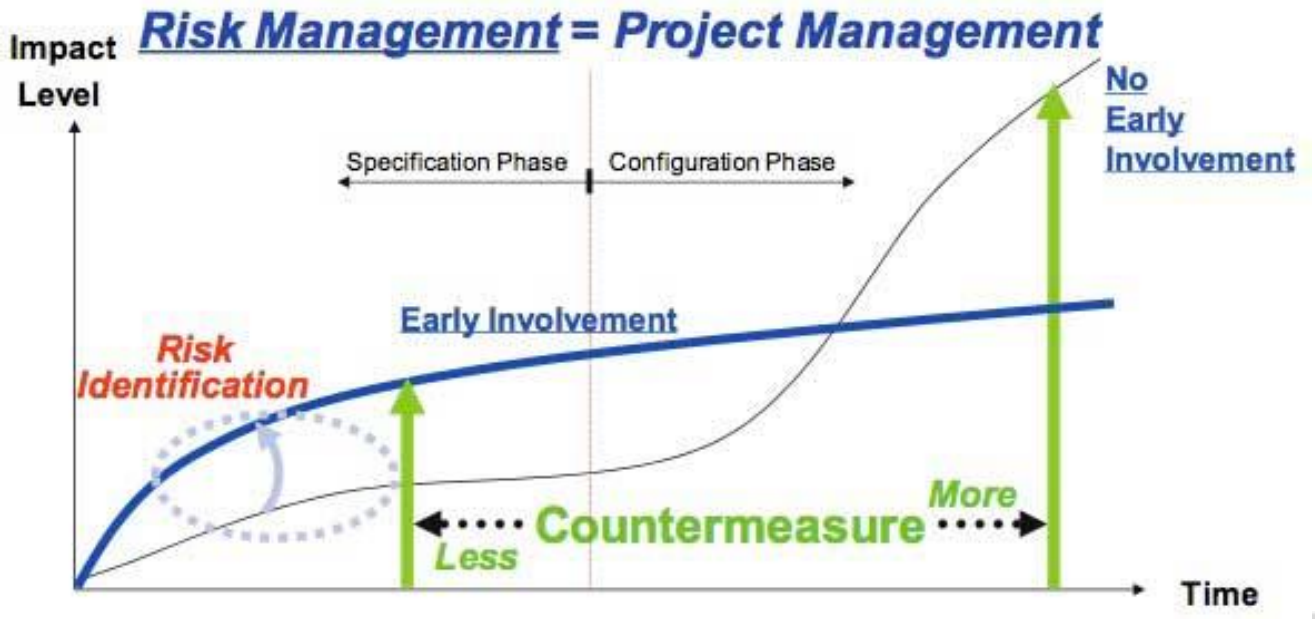
Early Supplier Involvement Benefits



- Early design interface and collaboration among designers, buyers, and suppliers throughout the product development cycle significant improves the ability to impact to the design.

- Identifying risks early enable customers to better manage their design

- Resulting overall lower project costs and higher **VALUE Products**



SMTC Corporation

THANK YOU

Engineering Work Plan

SMTC
Customer

Initial Design	DFX Engagement	Final DFX Review	Build Release	Quick-turn Mfg.	Build Delivery
▪ Design Services Engagement ▪ Technology Review ▪ BOM Scrub ▪ Lifecycle/ Risk Assessment ▪ Strategic Supplier Alignment	▪ BOM Scrub ▪ Lifecycle/ Risk Assessment ▪ Pre-Design for Assembly Review ▪ Pre-Design for Manufacturability Review	▪ AML Expansion ▪ Design for Fabrication ▪ Design for Assembly Review ▪ Design for Manufacturability Review ▪ Schematic, Nodal, Test Strategy Analysis	▪ NRE Ordered Stencils | Fixtures ▪ SMT, AOI, AXI and FP pre-programming	▪ Process Profile Development and Finalize Programming ▪ Invite Customer onsite ▪ SMT Top Side/Bottom Side + AOI/X-ray (1-2 days) ▪ Testing / Flying Probe, FQA (1-2days) ▪ System Level Integration ▪ Bring-Up or Test	▪ Provide Post Build DFX within 24-48 hours of completed shipment
Pre-Placement	**Routing**	**Gerber Files Released**	**PCB Fabrication**	**PCBA Production**	**Post Build Report**
2 days	**5 days**	**5 days**		**7 days**	**2 days**

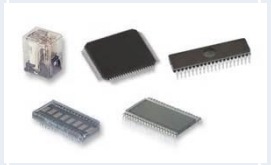
LEAD TIME
CYCLE TIME

Design Phase	Prototype Phase	Prototype Phase	Prototype Phase	Prototype Phase
▪ Requested Design Support ▪ Product Definition ▪ High-Level Design ▪ Areas for Development ▪ Cross-Checking DFX ▪ Costed BOM RFQ	▪ Preliminary Design ▪ Limited Routing ▪ Request for Pre-DFA ▪ Request for Pre-DFM	▪ Final routed design ▪ Pre-DFA/DFM findings reviewed/implemented ▪ Request for DFF ▪ Request for DFA ▪ Request for DFT/FEA	▪ Review and address critical DFx (as required)	▪ Receive Prototypes ▪ Request for Post-DFM/ Post Build Report

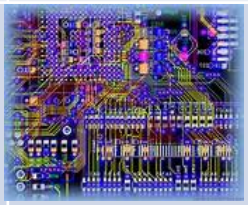
DFX Engagement Case Study

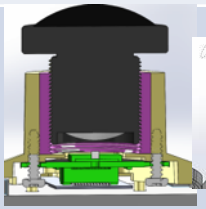
Examples

- **Design for Supply Chain (DFSC)**
- Perform BOM and Lifecycle Analysis to identify EOL and discontinued early in the procurement cycle.
- Supported last time buy and provided FFF alternates to support design
- Performed AML Expansion to provide cost savings and supply chain flexibility

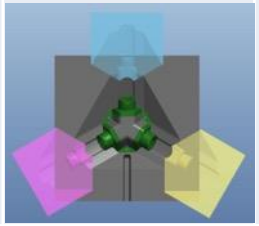


- **Design for Assembly (DFA)**
- Performed Stack up Tolerance and Interference Analysis to identify manufacturing and assembly issues.
- Performed Valor virtual part and DFM analysis of all printed circuit boards to identify assembly and design related issues.





- **Design for Manufacturability (DFM)**
- Incorporated early supplier involvement and DFM with key Metal, PCB and Plastic Suppliers
- Established manufacturing tolerances and capabilities into tolerance and stack up to provide critical dimensions to ensure function of final unit.



- **Design for Testability**
- Performed Board and System level schematic review
- Utilizing Test Expert performed Nodal access and Coverage Reporting
- Provided Test Strategy Analysis and Functional Recommendation

- **Design and Development**
- Combined Solidworks models and perform Analysis
- Re-layout flex cable to optimize via positions and decrease connector footprint
- Re-layout sensor board to move traces and address shorting issues
- Develop custom automated lens focusing and system level test fixture.